A Universal Grid-Connected Fuel-Cell Inverter for Residential Application

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Abstract—This paper describes a universal fuel-cell-based grid-connected inverter design with digital-signal-processor-based digital control. The inverter has a direct power conversion mechanism with a high-frequency zero-voltage-switched dc/ac primary-side converter followed by a pair of ac/ac cycloconverters that operates either in parallel or in series to simultaneously address the issues of universal output and high efficiency. The critical design issues focus on the impact and optimization of transformer leakage inductance with regard to effectiveness of zero voltage switching of a primary-side converter, duty-cycle loss, resonance, and voltage spike that has effect on the breakdown voltage rating of the cycloconverter devices. An additional concept of dynamic transformer tapping has been explored to address the impact of varying input voltage on secondary-side voltage spike and inverter efficiency. Finally, detailed grid-parallel and grid-connected results are presented that demonstrate satisfactory inverter performances.

Index Terms—AC/AC, control, dc/ac, digital signal processor (DSP), fuel cell, grid, high frequency, inverter, residential.

I. Introduction

THE utilization of fuel cells for distributed power generation requires the development of a low-cost, high-efficiency, and universal power-electronic system that converts a fuel cell's low-voltage output, which usually varies from 30 to 60 V for residential application, into commercial 120-V/60-Hz and 240-V/50-Hz ac outputs [1]–[3]. In addition, the power-electronic system should have the following characteristics: 1) output-voltage regulation for a wide variation in the output voltage of the fuel-cell stack; 2) capability for standalone and grid-connected operations; 3) low output harmonics; and 4) high energy-conversion efficiency.
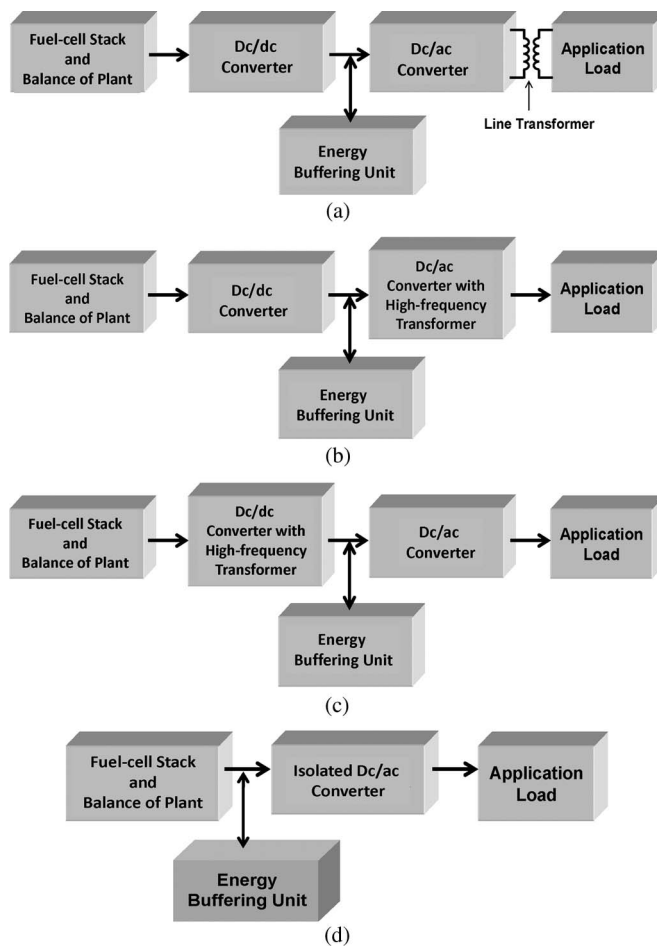

Fig. 1. Power-conditioning scheme with (a) line-frequency transformer, (b) high-frequency transformer in the dc/ac stage [7], (c) high-frequency transformer in the dc/dc stage [18], [19], and (d) single-stage isolated dc/ac converter [20].

Fig. 1(a)–(c) shows three mechanisms for achieving galvanic isolation between the fuel-cell stack and the application load. The conventional scheme, shown in Fig. 1(a), achieves isolation by placing a 50-Hz/60-Hz line-frequency transformer at the output of the inverter. Such a transformer is bulky because it has to handle low-frequency currents and voltages. The other two options, shown in Fig. 1(b) and (c), achieve isolation by placing the transformer within the power-conditioning system. The high-frequency isolation can be included in the dc/ac converter stage, as shown in Fig. 1(b) [7], or in the dc/dc converter stage, as shown in Fig. 1(c) [18], [19]. Fig. 1(d) shows an even more compact power-electronics option [20]. The single-stage isolated topology requires either a higher fuel-cell-stack
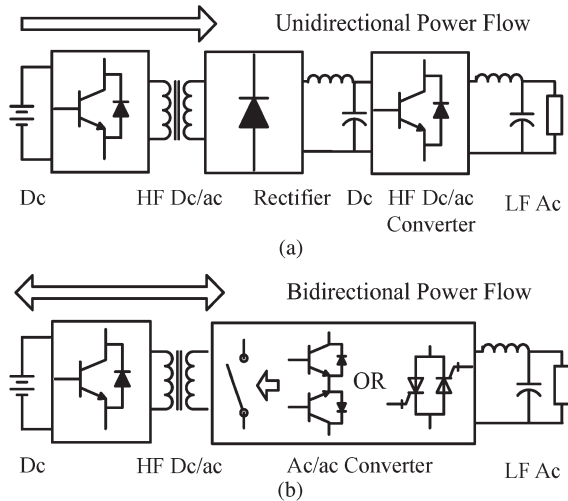
Fig. 2. Block diagram of high-frequency link inverter configurations: (a) dc/dc-type and (b) cycloconverter-type converter configurations.

voltage or slightly higher turns ratio of the transformer for a lower stack voltage to generate the needed 120-V/240-V line output. Overall, the isolation transformers for the schemes shown in Fig. 1(b)–(d) operate at high frequency and, hence, are significantly smaller than the line-frequency transformer shown in Fig. 1(a).

With regard to an isolated inverter, several topological configurations have been proposed to achieve fuel-cell power conversion at high efficiency without incurring high cost [1]–[10]. Based on where the transformer is inserted for isolating the stack from the load, these topologies can be broadly classified into two categories. The first one is referred to as the *"dc/dc-type converter"* and is shown in Fig. 2(a). It comprises a high-frequency dc/ac converter followed by a high-frequency transformer, a diode rectifier (inserted at the secondary of the transformer), and a link filter to obtain a higher dc voltage. Following this isolated dc/dc stage, a dc/ac converter is inserted to obtain a low-frequency ac. Because this type of topology has three power-conversion stages, it may not always be a suitable choice from efficiency and cost point of views because each of the power stages has to have very high efficiency. Furthermore, with increasing output power, the size and the cost of the dc-link filter attain significance.

The second topology, outlined in this paper and referred to as the *"cycloconverter-type converter,"* is shown in Fig. 2(b). This architecture supports bidirectional power flow and reduces system complexity by removing the rectifier and the dc-link filter. Galvanic isolation is achieved by embedding the transformer into the overall inverter, which usually comprises a two-level or higher level dc/ac converter followed by an ac/ac converter [1], [7], [8], [16].

Fig. 3 shows a circuit diagram of the proposed universal inverter with input voltage varying between 30 and 60 V. It comprises a phase-shifted full-bridge dc/ac converter as a common primary stage followed by two identical high-frequency step-up transformers and two forced ac/ac converters. Switches Q_1–Q_4 of the dc/ac converter are sinusoidally modulated to create a high-frequency ac voltage, which is converted into a 60-Hz/50-Hz line-frequency ac by a combination of the ac/ac

converters and the LC output filters. As shown in Fig. 3(a) and (b), for 120- and 240-V ac outputs, the two filter capacitors of the ac/ac converters are connected in parallel and in series, respectively.

Phase-shifted control of the dc/ac converter enables Q_1–Q_4 to be turned on under a zero-voltage-switching (ZVS) condition due to the resonance between the primary-side leakage inductance of the high-frequency transformer and the output capacitances of the MOSFETs [11]. Unlike the complex schemes outlined in the literature [9], [10], [12], which implement high-frequency switching for both the dc/ac converter and the ac/ac converter stages, the ac/ac converter switches in the control scheme outlined in this paper (see Figs. 16 and 17) are commutated primarily at line frequency when the polarities of output current and output voltage are the same and at high frequency when the polarities are opposite. Thus, under unity-power-factor operation, due to line-frequency switching, the ac/ac converter switching losses are significantly reduced.

Furthermore, unlike the topology outlined in [9] and [10], for an uninterruptible-power-supply application that usually has a high input voltage, in a fuel-cell-inverter application, owing to the low stack voltage, a step-up transformer with high turns ratio is necessary to obtain the rated ac output. For instance, for an input of 30 V, the primary-to-secondary turns ratio (N) of the transformer is calculated to be 13 to achieve the desired 240-V ac output. Fabrication of a 1-kW 1:13 high-frequency transformer is relatively difficult. Furthermore, high turns ratio yields enhanced secondary leakage inductance and secondary winding resistance, both of which result in a measurable loss in duty cycle and an increase in secondary copper loss. Higher leakage inductance also leads to higher voltage spike, which adds to the high nominal voltage of the secondary and necessitates the use of high-voltage power devices for the ac/ac converter. Such devices usually have higher on resistance and slower switching speeds, both of which diminish the overall system efficiency.

This paper addresses key design issues related to these challenges and proposes simple but effective solutions to improve efficiency. The focus of the design issues is on the effects of transformer leakage inductance on the ZVS and loss in the duty cycle of the dc/ac converter and on resonance, which results in voltage spike that affects the breakdown-voltage rating of the ac/ac converter devices. The concept of dynamic transformer tapping has been investigated to address the effects of input-voltage variation on voltage-spike mitigation and inverter efficiency. Subsequently, the control strategies for standalone and grid-connected operations and experimental design of a 1-kW inverter prototype are described. The experimental results and performances verify the effectiveness of the inverter and show its promising applications for fuel-cell as well as photovoltaic and battery-based power systems.

II. PRINCIPLES OF OPERATION

The basic schematic of the proposed universal inverter is shown in Fig. 4(a) and is used in the following sections to simplify the analysis. The ac/ac converters are switched based on output-voltage polarity, since primarily, unity-power-factor
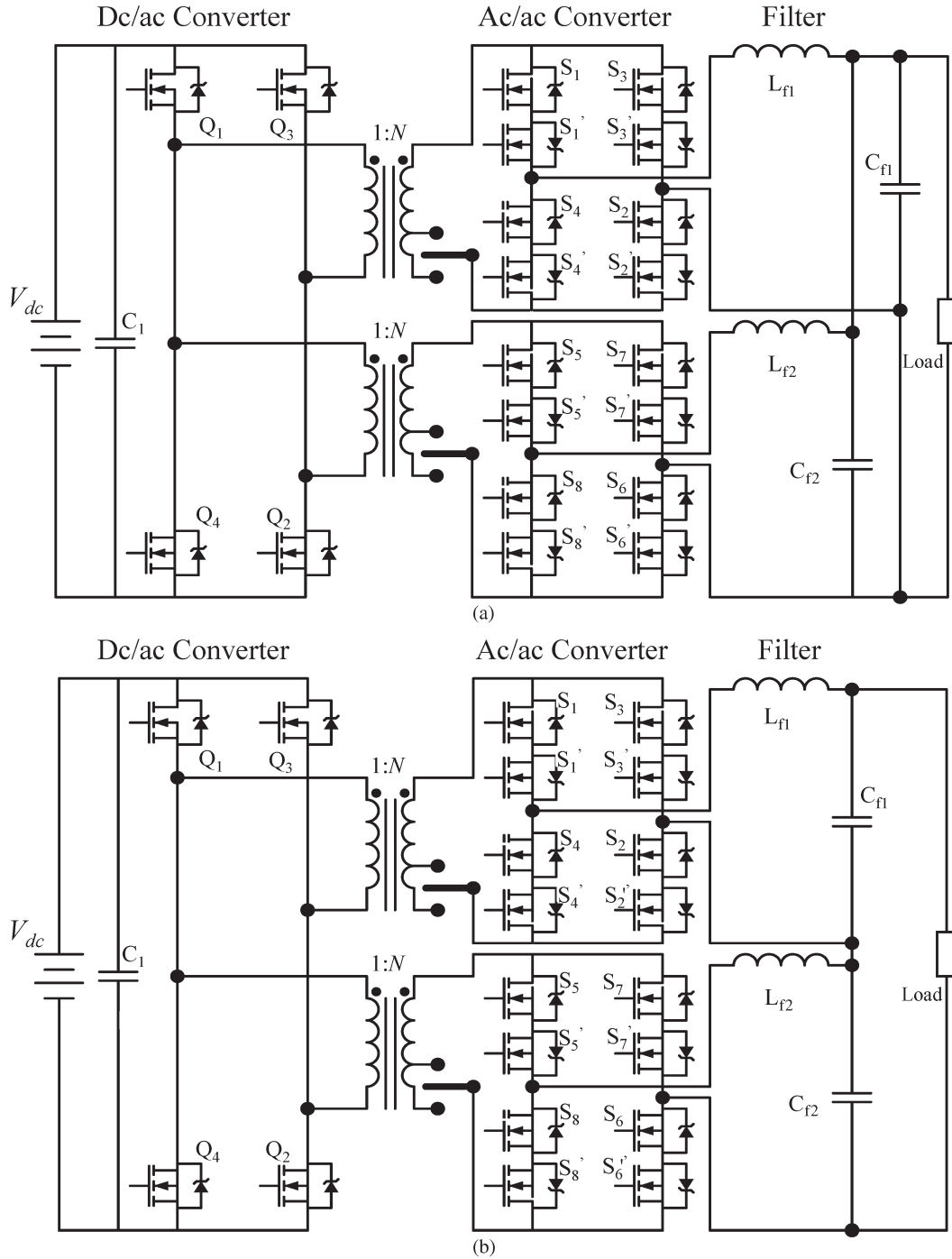
Fig. 3. Circuit diagrams of the proposed fuel-cell inverter for (a) 120-V/60-Hz ac and (b) 240-V/50-Hz ac outputs. An SPDT switch enables adaptive tapping of the transformer.

operation is required for the present design, and hence, the duration for which the polarities of the output voltage and current are different is negligibly small. The circuit schematic is the same as a conventional transformer-isolated full-bridge pulsewidth-modulation (PWM)-based dc/dc converter but has two different sets of rectifier arrangements for the positive and negative line cycles, as shown in Fig. 4(b) and (c). An illustration of the inverter operation is shown in Fig. 4(d), taking into account the two secondary-side ac/ac converters. Basically, the primary-side dc/ac converter is modulated to create a bipolar high-frequency waveform, which is amplified by the transformer and eventually shaped by the secondary-side ac/ac converters to generate the desired output ac waveform after passing the sinewave-modulated high-frequency signals through the output LC filter. Because the dc/ac converter creates the sinewave-modulated output, the ac/ac converter switches do not need to force switch; they can simply operate at line frequency to rectify the bipolar sinewave-modulated output. In practice, to preclude the reverse-recovery problem of the MOSFET, antiparallel diode, use of Schottky diode [21] or channel conduction of one of the MOSFETs [as shown in Fig. 4(d)] may need to be adopted.
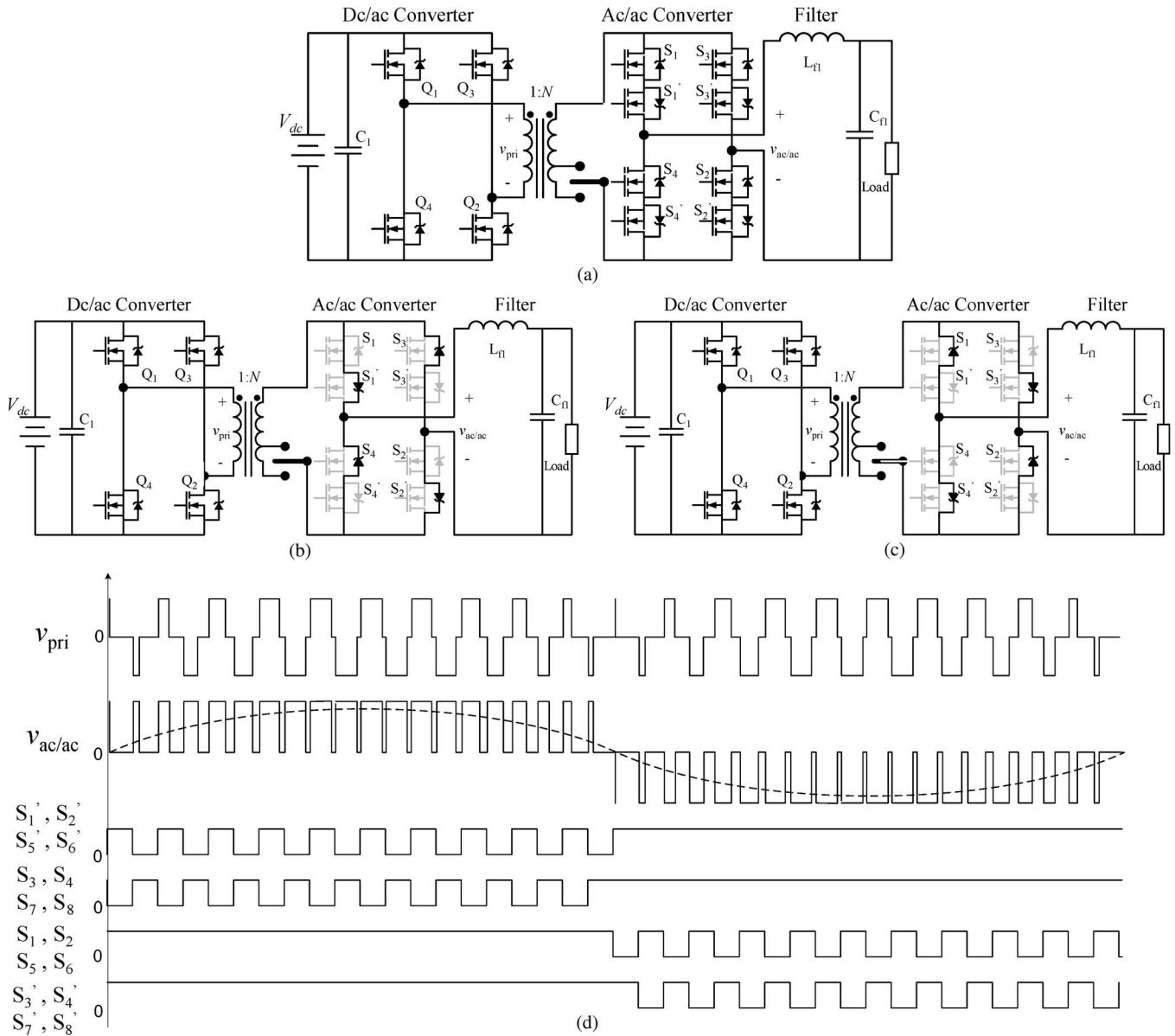
Fig. 4. (a) Circuit elements of the inverter. Power-stage circuits for (b) positive and (c) negative line cycles. (d) Gate-drive signals and key waveforms.

Next, we discuss the modes of operation for 120-V ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same. The rationale for a tapped transformer is provided in Section III-C. Fig. 5(f) shows the waveforms for the five operating modes of the dc/ac converter for positive primary and positive filter-inductor currents. Modes 2 and 4 show the ZVS turn-on mechanism for switches Q_4 and Q_3, respectively. Overall, the five modes of the inverter operation are discussed next for a positive primary current. A set of five modes exists for a negative primary current as well. A similar set of five modes of operation and corresponding circuit configurations for 240-V ac output is shown in Fig. 6 for input voltage above 42 V (corresponding to $N = 4.3$). Again, the mode of operation for input voltage below 42 V (corresponding to $N = 6.5$) remains the same.

Mode 1 [Fig. 5(a)]: During this mode, switches Q_1 and Q_2 of the dc/ac converter are on, and the transformer primary currents i_{pri1} and i_{pri2} are positive. The output current (i_{out}) splits equally between the two ac/ac converter modules. For the top ac/ac converter module, $i_{out}/2$ is positive and flows through the switches S_1 and S_1', the output filter L_{f1} and C_{f1}, switches S_2 and S_2', and the transformer secondary. Similarly, for the bottom ac/ac converter module, $i_{out}/2$ is positive and flows through the switches S_5 and S_5', the output filter L_{f2} and C_{f2}, switches S_6 and S_6', and the transformer secondary.

Mode 2 [Fig. 5(b)]: At the beginning of this interval, the gate voltage of Q_1 undergoes a high-to-low transition. As a result, the output capacitance of Q_1 begins to accumulate charge, while the output capacitance of Q_4 begins to discharge. Once the voltage across Q_4 goes to zero, it can

Fig. 5. Modes of operation for 120-V/60-Hz ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). (a)–(e) Topologies corresponding to the five operating modes of the inverter for positive primary and positive filter-inductor currents. (f) Schematic waveforms show the operating modes of the dc/ac converter when primary currents are positive. The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same.
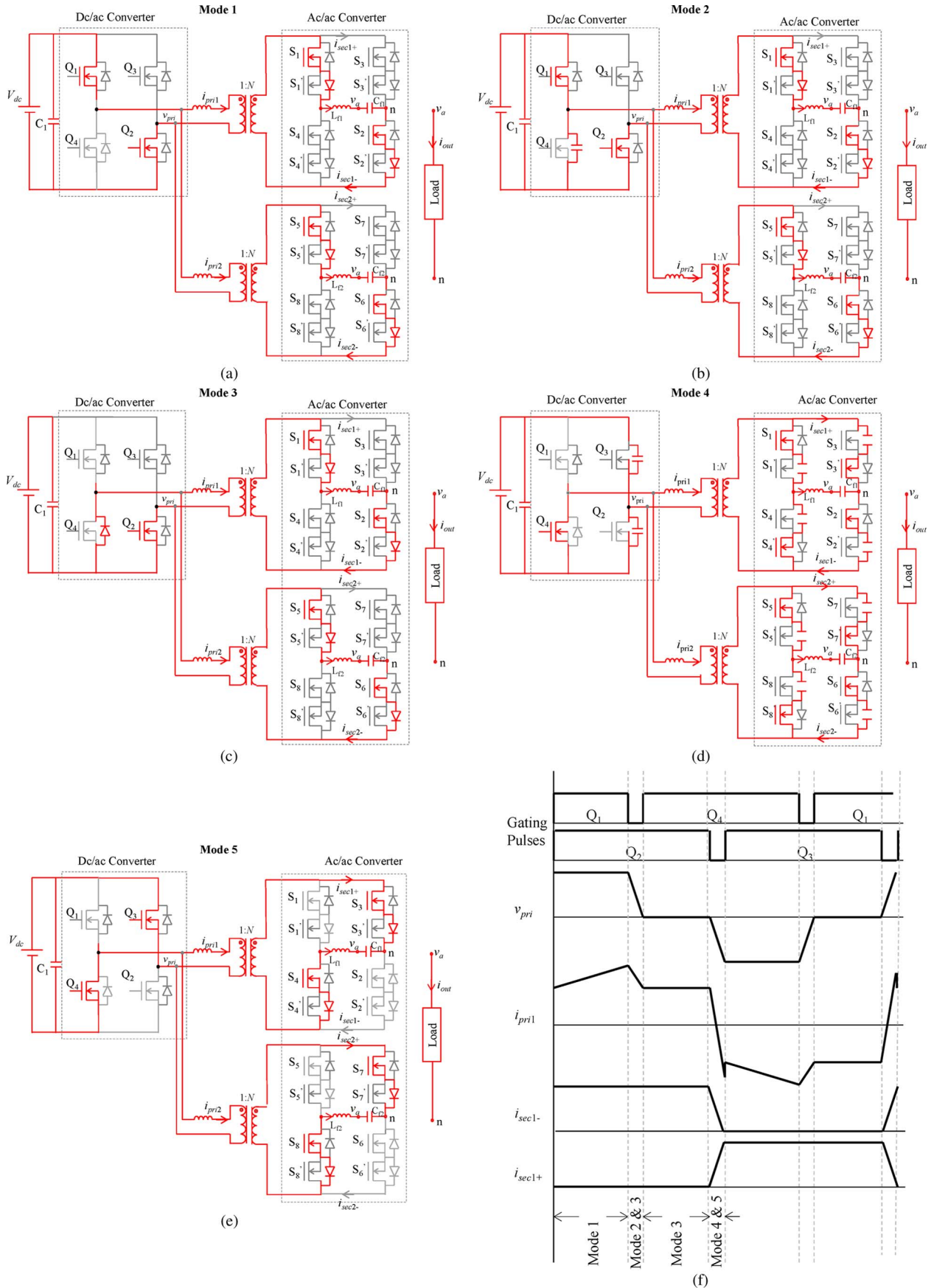
Fig. 6.   Modes of operation for 240-V/50-Hz ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). (a)–(e) Topologies corresponding to the five operating modes of the inverter for positive primary and positive filter-inductor currents. (f) Schematic waveforms show the operating modes of the dc/ac converter when primary currents are positive. The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same.
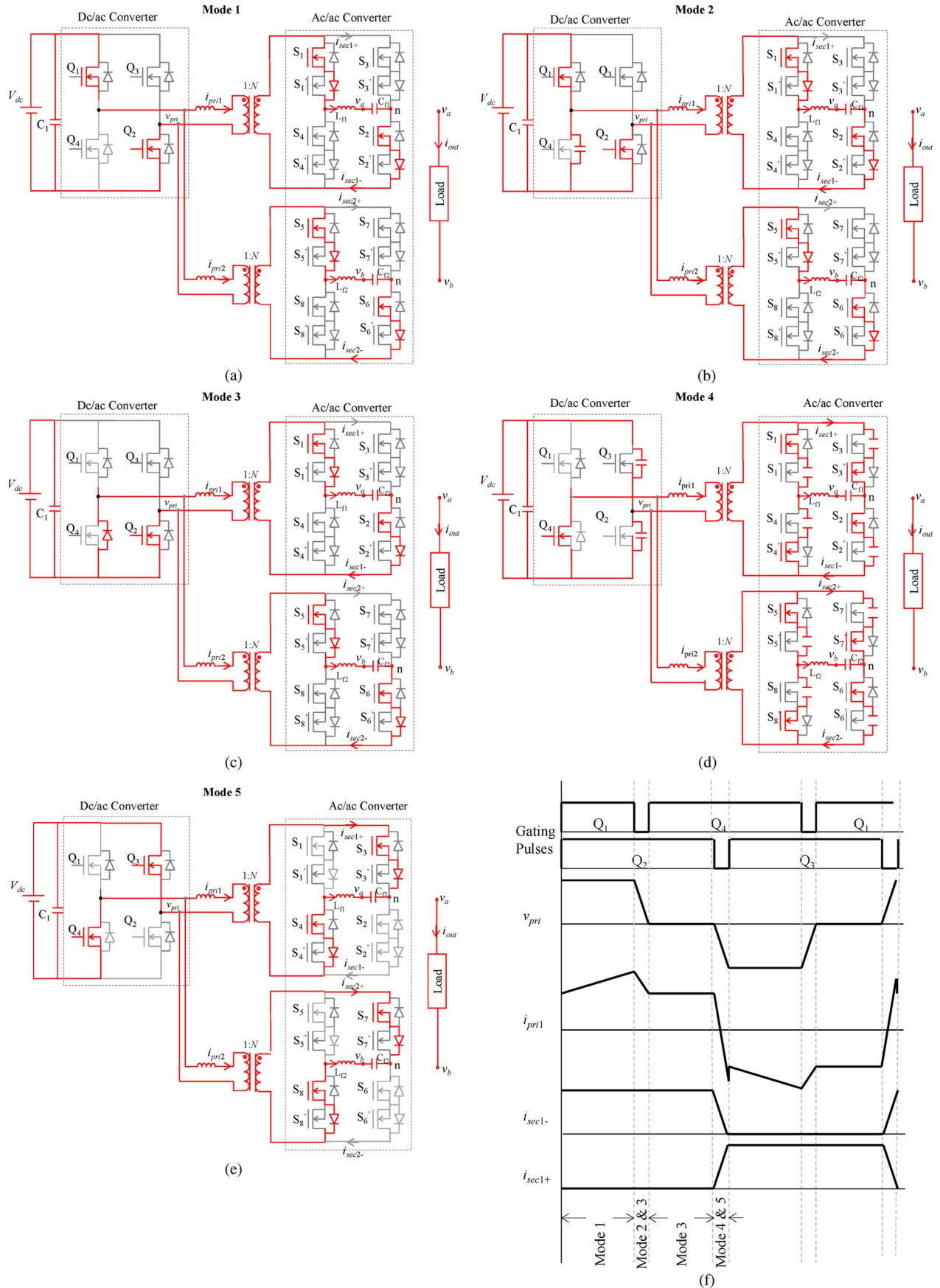
be turned on under ZVS. The transformer primary currents i_{pri1} and i_{pri2} and the load current i_{out} continue to flow in the same direction.

Mode 3 [Fig. 5(c)]: This mode initiates when Q_1 turns off. The transformer primary currents i_{pri1} and i_{pri2} are still positive and freewheel through Q_4 as shown in Fig. 5(c). Moreover, the load current continues to flow in the same direction as in Mode 2. Mode 3 ends when Q_2 starts to turn off.

Mode 4 [Fig. 5(d)]: At the beginning of this interval, the gate voltage of Q_2 undergoes a high-to-low transition. As a result, the output capacitance of Q_2 begins to accumulate charge, while the output capacitance of switch Q_3 begins to discharge, as shown in Fig. 5(d). The charging current of Q_2 and the discharging current of Q_3 together add up to the primary currents i_{pri1} and i_{pri2}. The transformer primary currents make a transition from positive to negative. Once the voltage across Q_3 goes to zero, it is turned on under ZVS condition. The load current flows in the same direction as in Mode 3 but makes a rapid transition from the bidirectional switches S_1 and S_1' and S_2 and S_2' to S_3 and S_3' and S_4 and S_4'. During this process, $i_{\mathrm{out}}/2$ splits between the two legs each of the ac/ac converter modules as shown in Fig. 5(d). Mode 4 ends when the switch Q_2 is completely turned off and its output capacitance is charged to V_{dc}. At this point, it is necessary to note that, because S_1 and S_2 and S_5 and S_6 are off simultaneously, each of them supports a voltage of V_{dc}.

Mode 5 [Fig. 5(e)]: This mode starts when Q_2 is completely turned off. The primary currents i_{pri1} and i_{pri2} are negative, while the load current is positive as shown in Fig. 5(e).

Finally, and as shown in Fig. 4, there are always two MOSFET body diodes conducting current in each ac/ac converter, and the high-frequency ac voltage at the input of the ac/ac converter forces current commutation back and forth between one set of MOSFET diodes and the other. For instance, the MOSFET body diodes of the top ac/ac converter will switch alternately between S_1' and S_2' and S_3 and S_4 during the positive line cycle and between S_1 and S_2 and S_3' and S_4' during the negative line cycle. The enhanced efficiency of the ac/ac converter, realized due to line-frequency switching of the MOSFETs, is partially offset by the relatively higher forward-voltage drop and inefficient reverse-recovery characteristics of the MOSFET body diodes. External antiparallel diodes with lower voltage drop and faster reverse recovery will reduce the loss, thereby improving the efficiency.

The substitution of the MOSFET body-diode conduction by channel conduction of the MOSFET is another solution, which precludes the need for adding multiple external diodes in parallel. As shown in Fig. 4(d), the MOSFETs, which are previously turned on during a half-a-line cycle, will remain in the same state, while the MOSFETs previously in the off state will switch on and off to provide corresponding current paths along with their body diodes according to the polarity of high-frequency ac-link voltage. Majority of the current will flow through the lower resistance path of the MOSFET channels in the direction either from drain to source or from source to drain.
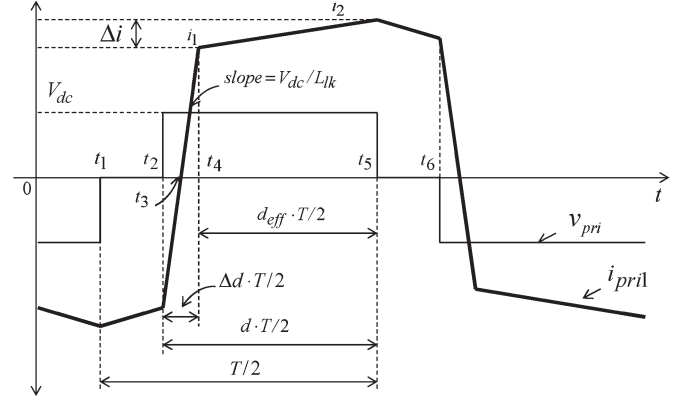

Fig. 7. Transformer primary-side voltage and current waveforms for the circuit shown in Fig. 3.

The body diodes of the MOSFETs will share a smaller amount of current. Compared with the body diode, the MOSFET channel usually has less on-state drop and enables faster switching speed. Consequently, the conduction and the switching losses will be relatively lower. However, synchronization of gate-drive signals between the dc/ac converter and the ac/ac converter switches is necessary in this case, which is realized by using the gate-drive signal of Q_1 and its complementary signal for controlling the ac/ac converter switches.

The switching pattern of the ac/ac converter, as shown in Fig. 4(d), was implemented, and its efficacy was verified via experimental tests on the inverter prototype. Approximately 1%–2% improvement in energy-conversion efficiency was obtained over the entire output power range by primarily enabling MOSFET-channel conduction instead of body-diode conduction.

III. DESIGN ISSUES

A. Duty-Ratio Loss

Fig. 7 shows one cycle of the primary-side high-frequency voltage and current waveforms for a conventional dc/dc converter [11]. Note that a significant difference between the operations of a dc/dc and a dc/ac converter is that the phase-shift angle of the former is controlled by a dc signal while it is modulated by a sinusoidal signal for the latter. The finite slope of the rising and falling edges of a transformer primary current due to the leakage inductance (L_{lk}), as shown in Fig. 7, will reduce the duty cycle (d). The duty-ratio loss is expressed as

$$\Delta d = \frac{i_1 + i_2}{\left(\frac{V_{\mathrm{dc}}}{L_{lk}}\right) \cdot \left(\frac{T}{2}\right)} \tag{1}$$

where

$$i_1 = N \cdot (i_{\mathrm{out}} - \Delta i/2) \tag{2}$$

$$i_2 = N \cdot \left(i_{\mathrm{out}} + \Delta i/2 - \frac{v_{\mathrm{out}}}{L_{f1}} \cdot (1 - d) \cdot T/2\right) \tag{3}$$

$$i_{\mathrm{out}} = \frac{\sqrt{2}P_{\mathrm{out}}}{v_{\mathrm{out}}\cos(\phi)}. \tag{4}$$
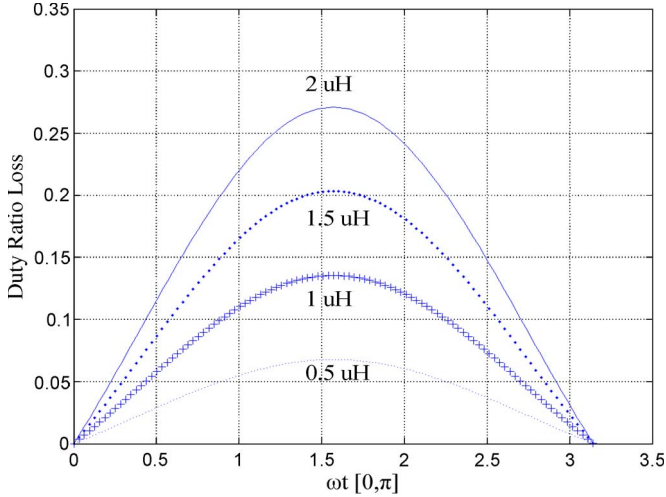
Fig. 8.   Variation of the duty-ratio loss as a function of the leakage inductance of the transformer over the half-a-line cycle.

TABLE I
CONDUCTING COMPONENTS AT DIFFERENT INTERVALS FOR
THE CIRCUIT SHOWN IN FIG. 4(a). DIODES D_1-D_4
ARE ANTIPARALLEL DIODES OF Q_1-Q_4

Interval	Conducting Components
$t_1 \sim t_2$	D_1, Q_3
$t_2 \sim t_3$	D_1, D_2
$t_3 \sim t_4$	Q_1, Q_2
$t_4 \sim t_5$	Q_1, Q_2
$t_5 \sim t_6$	Q_2, D_4

In (2) and (3), N is the transformer turns ratio, L_{f1} is the output filter inductance, i_{out} is the filter current, v_{out} is the output voltage, T is the switching period, Δi is the filter inductor current ripple, P_{out} is the output power, and $\cos(\phi)$ is the load power factor. By substituting (2) and (3) into (1), we obtain

$$\Delta d = \frac{N}{\frac{V_{dc}}{L_{lk}} \cdot \frac{T}{2}} \cdot \left(2i_{out} - \frac{v_{out}}{L_{f1}} \cdot (1-d) \cdot \frac{T}{2} \right). \quad (5)$$

Unlike the dc/dc converter, the duty-ratio loss is time varying for the dc/ac converter due to the sinusoidal nature of v_{out}, i_{out}, and d. Assuming that L_{f1} is large enough, the second term within the parenthesis of (5) can be omitted. Thus, the duty-ratio loss has a sinusoidal shape and is proportional to N and L_{lk}. One can deduce from (5) that, due to the high turns ratio and low input voltage, even a small leakage inductance will cause a big duty-ratio loss.

Fig. 8 shows the calculated duty-ratio loss for a 1-kW inverter prototype for an input voltage of 30 V and for $N = 6.5$. Four parametric curves corresponding to four leakage inductances of 0.5, 1, 1.5, and 2 μH are shown. Fig. 8 shows that, for a leakage inductance of 2 μH, the duty-ratio loss is more than 25%. Consequently, a transformer with even higher turns ratio is required to compensate for this loss in the duty ratio, which increases the conduction loss and eventually decreases the efficiency as explained hereinafter.

The conducting components of the dc/ac converter during the half switching cycle (i.e., for duration $t_1 \sim t_6$) are listed in Table I. The equations to calculate conduction losses for the
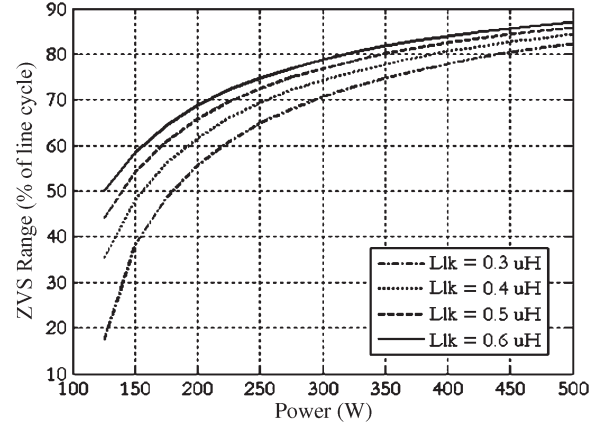

Fig. 9.   ZVS range of the dc/ac converter with variation in output power.

dc/ac converter switches can be simplified, provided that L_{f1} is large enough (i.e., i_1 equals i_2)

$$P_{Q1,4} = R_{on} \cdot \left(\left(\frac{i_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta d}{2} + i_1^2 \cdot d_{eff} \right) \quad (6)$$

$$P_{Q2,3} = R_{on} \cdot \left(\left(\frac{i_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta d}{2} + i_1^2 \cdot d_{eff} + i_1^2 \cdot (1-d) \right) \quad (7)$$

$$P_{D2,3} = \frac{i_1}{2} \cdot V_F \cdot \frac{\Delta d}{2} \quad (8)$$

$$P_{D1,4} = V_F \cdot \left(\frac{i_1}{2} \cdot \frac{\Delta d}{2} + i_1 \cdot (1-d) \right) \quad (9)$$

where V_F is the body-diode forward voltage drop of Q_1-Q_4, R_{on} represents their on resistances, and

$$d_{eff} = \frac{d}{\left(1 + 4 \frac{L_{lk}}{R_{load}} N^2 f_{SW} \right)}. \quad (10)$$

In (10), f_{SW} is the switching frequency of the dc/ac converter. From the aforementioned equations, it can be concluded that higher transformer leakage inductance yields lower value of effective duty ratio (d_{eff}). Therefore, to obtain the same output voltage, Δd [as described by (5)] increases to compensate for the reduction in d_{eff}, which results in a higher conduction loss. For the 1-kW inverter prototype under consideration, a combination of two transformers and two ac/ac converters on the secondary side of the high-frequency transformer is identified to be an optimum solution.

B. Optimization of the Transformer Leakage Inductance

The leakage inductance of the transformer aids in improving the ZVS range of the dc/ac converter but reduces the duty ratio of the converter that increases the conduction loss. Thus, the leakage inductance of each high-frequency transformer is designed to achieve the highest efficiency, as shown in Fig. 9.

For the sinusoidally modulated dc/ac converter, the ZVS capability is lost twice in every line cycle. The extent of the

loss of ZVS is a function of the output current. The available ZVS range (t_{ZVS}) as a percentage of the line cycle ($t_{LineCycle}$) is given by

$$\frac{t_{ZVS}}{t_{LineCycle}} = \frac{2}{\pi} \sin^{-1} \left(\frac{1}{4} \frac{V_{dc}^2 \left(\frac{4}{3} C_{oss} + \frac{1}{2} C_T \right)}{i_{out}^2 L_{lk}} \right)^{\frac{1}{2}} \quad (11)$$

where C_{oss} is the device output capacitance and C_T is the interwinding capacitance of the transformer. When the dc/ac converter is not operating under ZVS condition, the devices are hard switched. In steady state, the switching loss (P_{SW}) of each MOSFET during hard switching depends on the switching frequency and the gate resistance (R_{GATE}) and is given by

$$P_{SW} = \frac{V_{dc} i_{out} \sin(\omega t)}{2} f_{SW} \left(t_{S(L \to H)} + t_{S(H \to L)} \right) \quad (12)$$

where ω is the line frequency in radians per second and the low-to-high and high-to-low transition times ($t_{S(L \to H)}$ and $t_{S(H \to L)}$) are given by

$$t_{S(L \to H)} = \frac{Q_{G(SW)} R_{GATE}}{V_{DD} - V_{SP}} \quad t_{S(H \to L)} = \frac{Q_{G(SW)} R_{GATE}}{V_{SP}}. \quad (13)$$

In (13), $Q_{G(SW)}$ is the gate charge, V_{DD} is the bias voltage of the gate driver, V_{SP} is the source voltage, and R_{GATE} is the gate resistance. The conduction loss of the MOSFET in steady state is described using

$$P_{cond1,3} = R_{on} \left[\left(\frac{i_1 \sin(\omega t)}{\sqrt{3}} \right)^2 \frac{\Delta d}{2} + i_{out}^2 \sin^2(\omega t) d_{eff} \right] \quad (14)$$

$$P_{cond2,4} = R_{on} \left[\left(\frac{i_1 \sin(\omega t)}{\sqrt{3}} \right)^2 \frac{\Delta d}{2} + i_{out}^2 \sin^2(\omega t) d_{eff} \right.$$

$$\left. + i_1^2 \sin^2(\omega t)(1 - d) \right]. \quad (15)$$

To optimize the leakage inductance, the total loss of the dc/ac converter over the half-a-line cycle has to be estimated, and it is determined using

$$P_{device} = \frac{1}{\pi} \int_0^{\pi/\omega} \left(2P_{cond1,3} + 2P_{cond2,4} + 2P_{SW} \frac{t_{ZVS}}{t_{LineCycle}} \right) dt. \quad (16)$$

A numerical calculation of the total switching losses, as shown in Fig. 10, indicates that the optimal primary-side leakage inductance for the high-frequency transformer should be between 0.2 and 0.7 μH.

C. Transformer Tapping

The voltage variation on the secondary side of the high-frequency transformer necessitates high breakdown-voltage
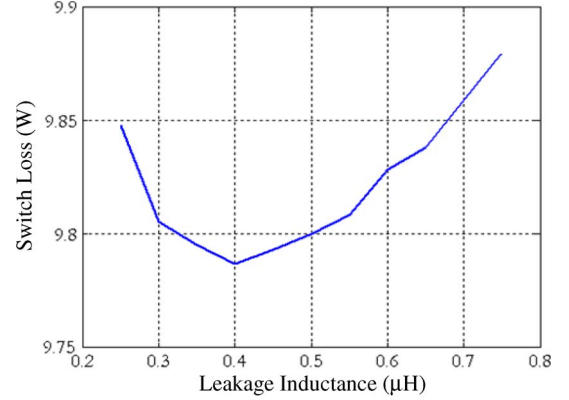

Fig. 10. Variation of the total switch loss of the dc/ac converter (for an output power of 500 W) with the leakage inductance of the high-frequency transformer. As the leakage inductance of the high-frequency transformer increases, the total switching loss decreases due to an increase in the range of ZVS, while the total conduction loss increases with increasing leakage inductance.
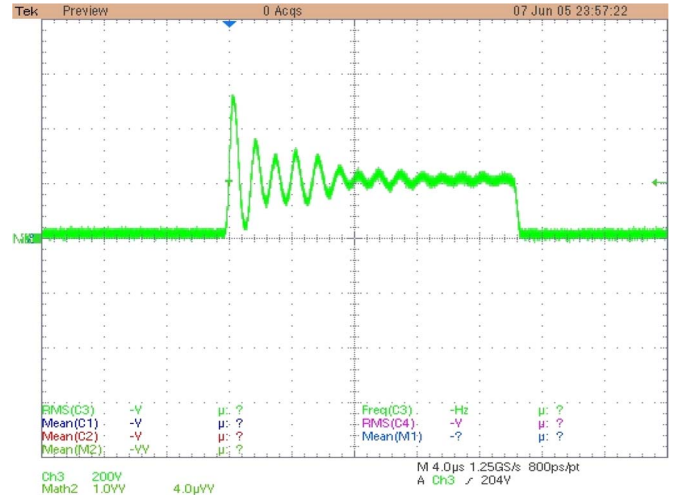

Fig. 11. Drain–source voltage across one of the ac/ac converter MOSFETs.

rating for the ac/ac converter switches and diminishes their utilization. For a step-up transformer with $N = 6.5$, the ac/ac converter switches have to withstand at least 390-V nominal voltage when input ramps to the high end (60 V), while only 195 V is required when 30 V is the input. In addition to the nominal voltage, the switches of the ac/ac converter have to tolerate the overshoot voltage (as shown in Fig. 11) caused by the oscillation between the leakage inductance of the transformer and the junction capacitances of the MOSFETs during turn-off [11]. The frequency of this oscillation is determined using

$$f_{ring} = \frac{1}{2\pi \sqrt{N^2 L_{lk} C_{eq}}} \quad (17)$$

where C_{eq} is the equivalent capacitance of the switch output capacitance and the parasitic capacitance of the transformer winding. The conventional passive snubber circuit or active-clamp circuits can be used to limit the overshoot, but they will induce losses and increase system complexity and component
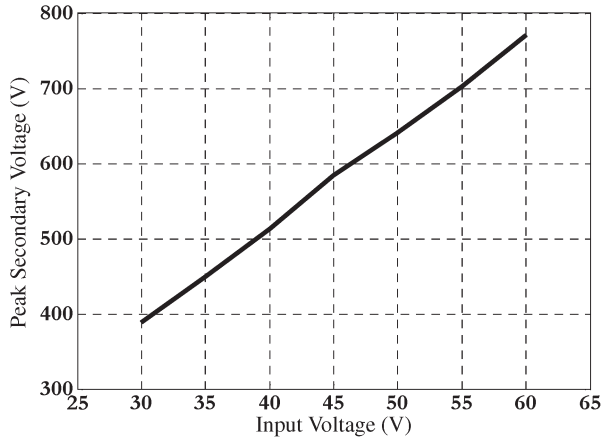
Fig. 12. Peak voltage across the ac/ac converter with varying input voltage for a transformer primary leakage inductance of 0.7 μH, output capacitance of 240 pF (for the devices of the ac/ac converter), and output filter inductance and capacitance of 1 mH and 2.2 μF, respectively.
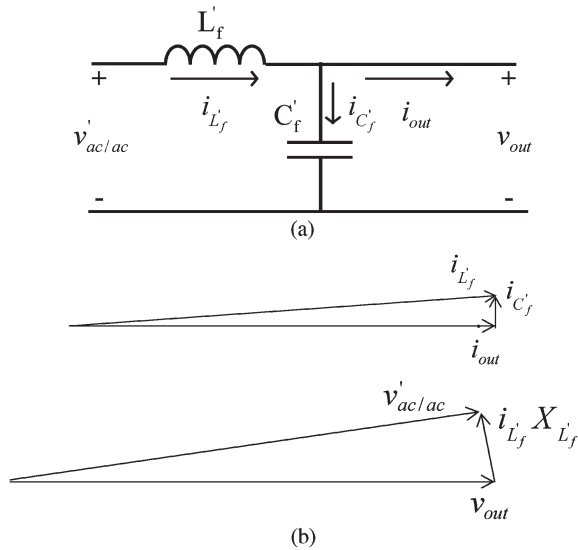

Fig. 13. (a) Schematic of the LC filter for standalone operation of the fuel-cell inverter. (b) Phasor diagram describing the relationship among voltages and currents of the LC filter. Symbols $v'_{ac/ac}$, L'_f, and C'_f represent the equivalent output voltage of the ac/ac converter and the equivalent filter inductance and capacitance for 120- and 240-V ac output operations.

costs. One simple but effective solution is to adjust the transformer turns ratio according to the input voltage.

To change the turns ratio of the high-frequency transformer, a bidirectional switch is required. Considering its simplicity and low conduction loss, a low-cost single-pole-double-throw (SPDT) relay is chosen for the inverter prototype, as shown in Fig. 3(a) and (b). For this prototype, for an input voltage in the range of 30–42 V, N equals 6.5. Hence, 500-V devices are used for the highest input voltage considering an 80% overshoot in the drain-to-source voltage that was observed in experiments. For an input voltage above 42 V, N equals 4.3, and hence, the same 500-V devices can still be used to cover the highest voltage as the magnitude of the voltage oscillation is reduced. The relay is activated near the zero-crossing point (where power transfer is negligible) to reduce the inrush current. Such an

Fig. 14. Two filter designs (along with their respective phasor diagrams) for the grid-connected inverter using (a) an L and (b) an LCL filter, connected between the inverter and the grid. Symbols $v'_{ac/ac}$, L'_f, and C'_f represent the equivalent output voltage of the ac/ac converter and the equivalent filter inductance and capacitance for 120- and 240-V ac output operations. Symbol L_{f3} represents the inductance between the grid and the inverter.

Fig. 15. Schematics of the converters for (a) the standalone and (b) grid-connected modes of operation. An SPDT relay is used to switch between the two modes of operation.

Fig. 16.   Schematic of the voltage-mode controller for standalone operation of the inverter.

arrangement improves the efficiency of the transformer and significantly increases the utilization of the ac/ac converter switches for the full range of the input voltage. On the other hand, without adaptive transformer tapping, the minimal voltage rating for the devices is given by
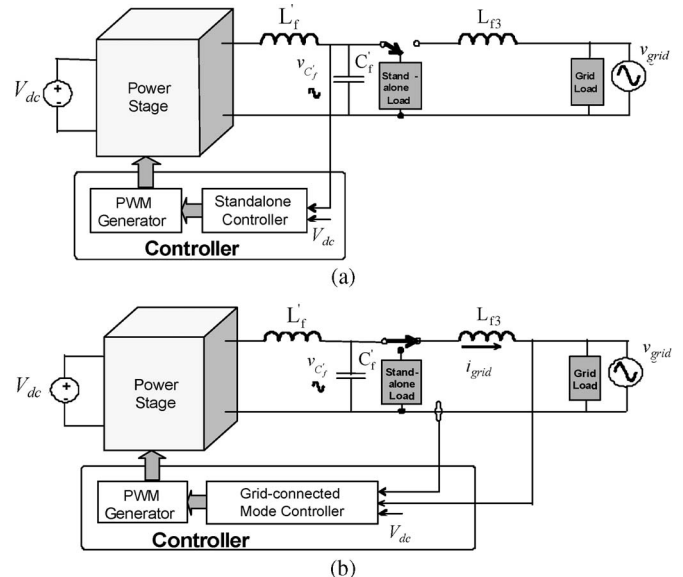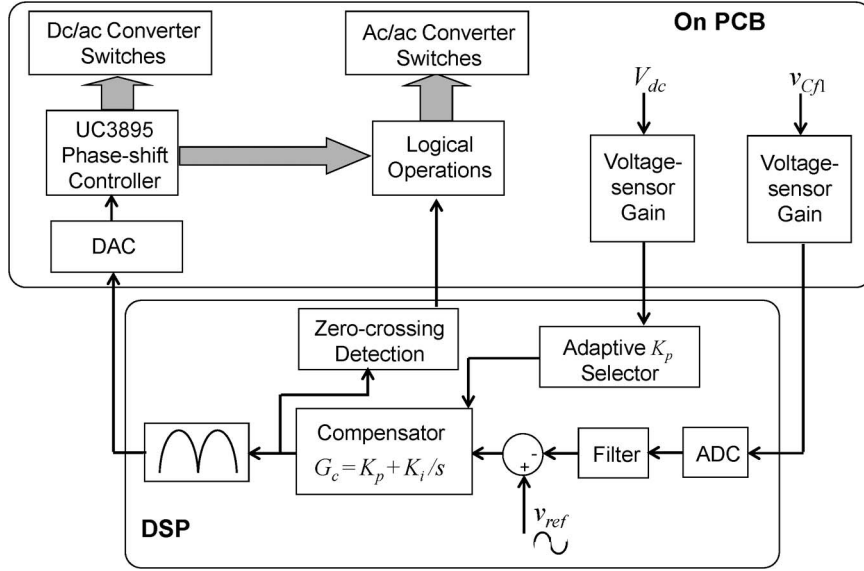
$$V_{\mathrm{dc_{max}}} \cdot N \cdot (1 + 80\%) = 60 \cdot 6.5 \cdot 1.8 = 702 \text{ V}. \qquad (18)$$

In practice, MOSFETs with 800 V or higher breakdown-voltage ratings are therefore required due to the lack of 700-V rating devices. The so-called rule of "silicon limit" (i.e., $R_{\mathrm{on}} \propto BV^{2.5}$, where BV is the breakdown voltage) indicates that, in general, higher voltage rating MOSFETs will have higher R_{on} and hence higher conduction losses. It is noted that the exponent of BV can be different for other power semiconductor devices such as CoolMOS. Furthermore, for the same current rating, the switching speed of a MOSFET with higher breakdown voltage rating is usually slower. As such, if one uses a MOSFET with 800 V or higher voltage rating, converter efficiency is expected to degrade further due to enhanced power loss.

D. Effects of Resonance Between the Transformer Leakage Inductance and the Output Capacitance of the AC/AC Converter Switches

Resonance between the transformer leakage inductance and the output capacitance of the ac/ac converter devices causes the peak device voltage to exceed the nominal voltage (obtained in the absence of the transformer leakage inductance). This is shown in Fig. 12. Considering $N = 6.5$, one can observe that the peak secondary voltage can be around twice the nominal secondary voltage. Consequently, the breakdown-voltage rating of the ac/ac converter switches needs to be higher than the nominal value. As MOSFETs are used as switches, higher breakdown voltage entails increased on resistance that yields higher conduction loss. Thus, the *leakage*

affects the conduction loss and selection of the devices for the ac/ac converter.

The resonance begins only after the secondary current completes changing its direction and the ac/ac converter switches initiate turn-on or turn-off. During this resonance period, energy is transferred back and forth between the leakage and filter inductances and device and filter capacitances in an almost-lossless manner. The current through the switch, which supports the oscillating voltage, is almost zero. Thus, practically, no switching loss is incurred due to this resonance phenomenon, although it may have an impact on the electromagnetic-emission profile.

E. Output Filter Design for the Standalone and Grid-Connected Inverter

For the fuel-cell inverter, the design of the output filter is critical. The filter is so designed such that it mitigates the high-frequency components of the output of the ac/ac converter and generates a sinusoidal voltage and current that satisfies the total-harmonic-distortion (THD) requirements. For the standalone operation of the inverter, we choose a second-order filter whose phasor diagram is shown in Fig. 13. The value of the filter inductor is chosen to meet the current ripple requirement according to the IEEE 519 standard and is given by [13]

$$L'_f > \frac{1}{8} \frac{NV_{\mathrm{dc}}}{0.2(i_{\mathrm{out}})f_{\mathrm{SW}}}.$$

Fig. 13 shows that the current $(i_{C'_f})$ through C'_f increases the reactive power drawn from the converter, which has an adverse effect on the efficiency of the fuel-cell inverter. The current through the capacitor is given by $i_{C'_f} = v_{\mathrm{out}}/\omega C'_f$, which shows that, if the capacitance is high, the amount of reactive current drawn from the inverter increases. The capacitance design is a tradeoff between the THD requirements and the tolerable reactive power drawn by the system. To meet the
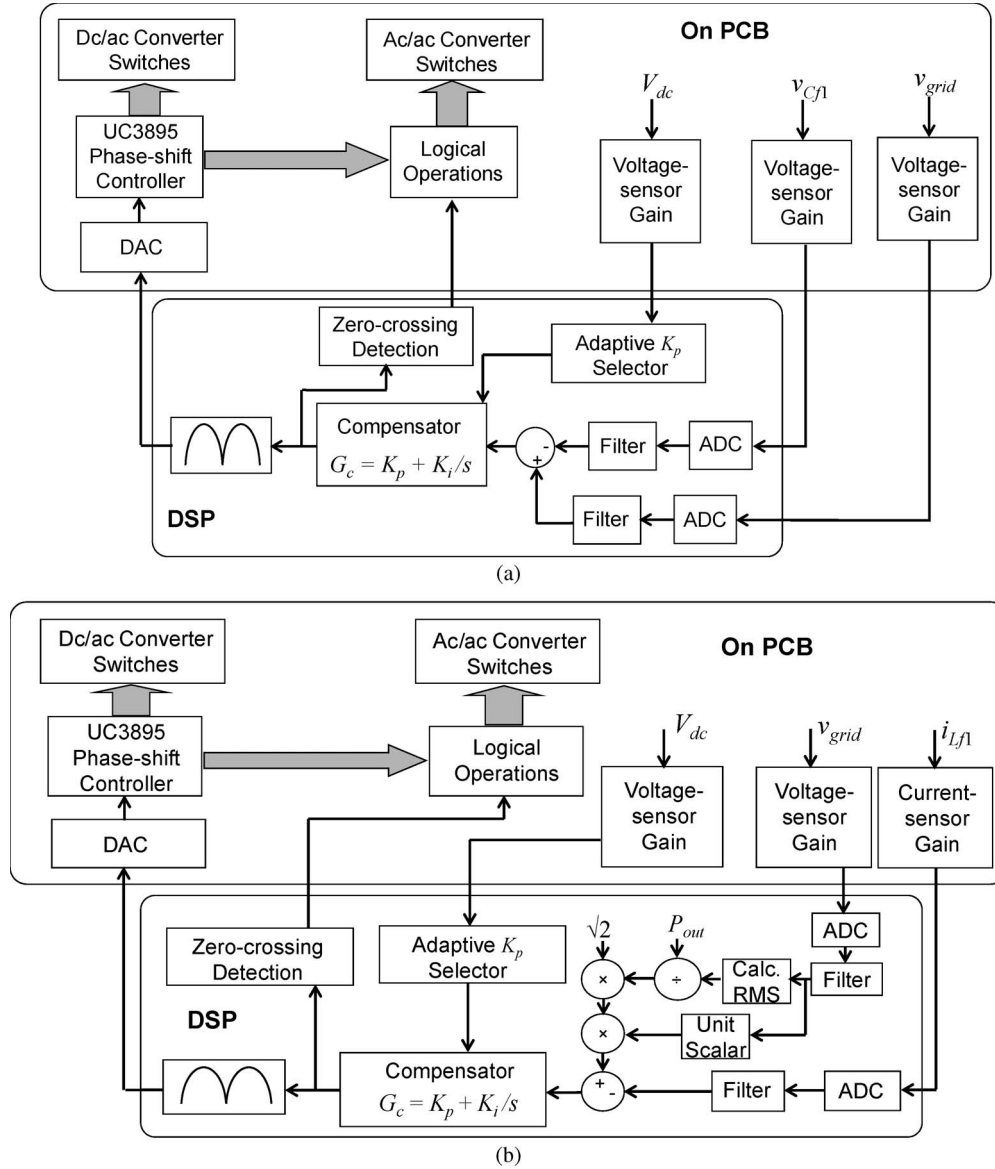
Fig. 17. (a) Schematic of the voltage-mode controller for the standalone inverter just before grid connection. (b) Schematic of the current-injection controller for the inverter after it is connected to the grid.

requirements of the IEEE 519 standard, the value of the filter capacitance is chosen to be [13]

$$C'_f = (\%P_{\text{Reactive}}) \frac{P_{\text{outrated}}}{\omega v_{\text{out}}^2}$$

where $\%P_{\text{Reactive}}$ is the tolerable reactive power and P_{outrated} is the rated output power of the inverter.

For the grid-connected operation, the inverter should have an inductive output to minimize the inrush current between the grid and the inverter. In Fig. 14, we outline two possible choices: a single-inductor (L) and an inductive–capacitive–inductive (LCL) filter. In [14] and [15], a simple L filter is proposed for the grid connection. However, to meet the regulatory standards of IEEE 519 or IEC 61000-3-2, the size of such an inductor has to be significantly large. This is mainly because the inductor has to bypass the higher order harmonics of the ac/ac output. Hence, we choose an LCL filter, as shown

TABLE II
SOME KEY DESIGN SPECIFICATIONS FOR THE INVERTER [1], [2]

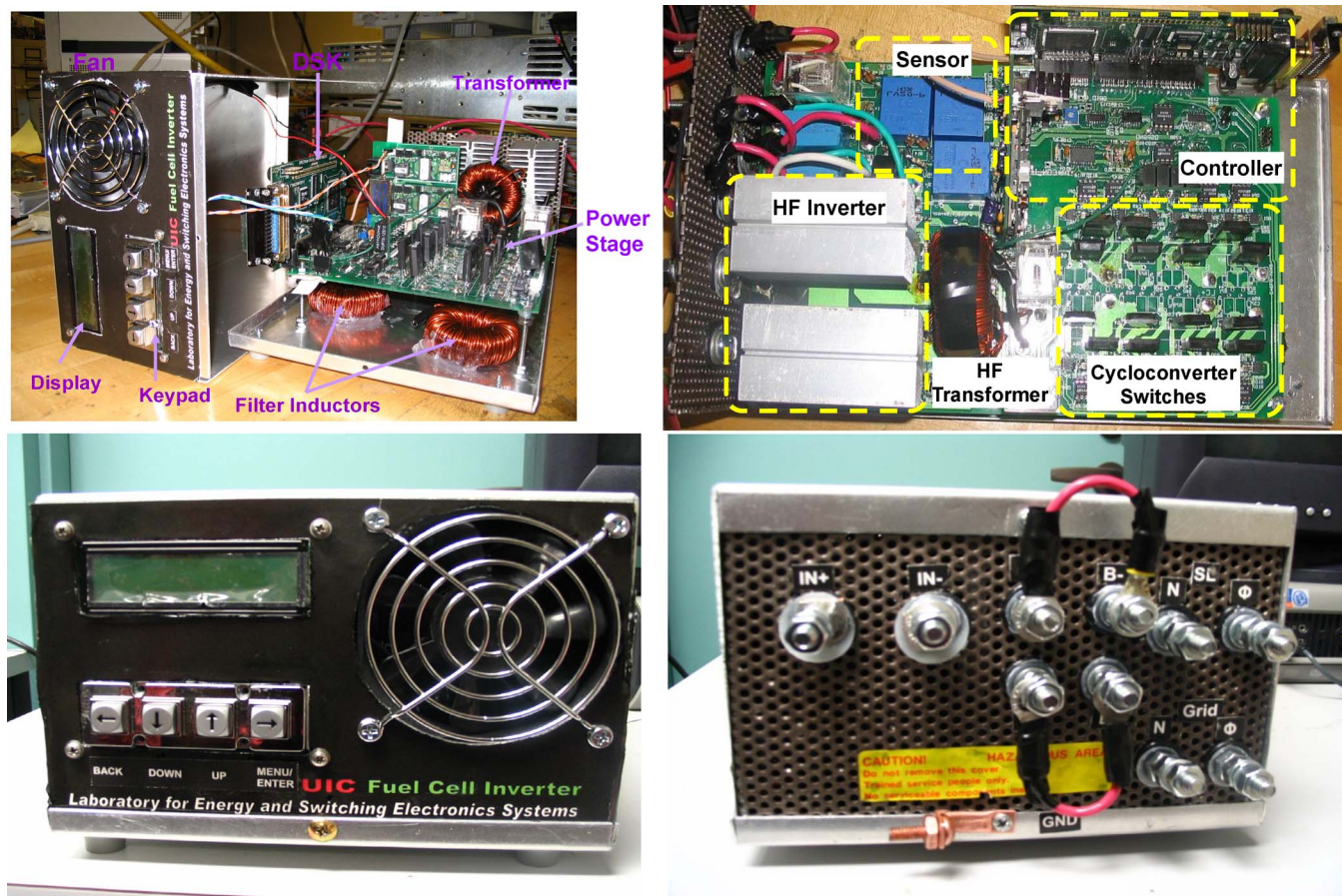| Input Source	30-60 V dc
Output Power	Up to 1 kW continuous, 3 kW for 20 line cycles
Output Voltage	120 V/60 Hz and 240 V/50 Hz ac outputs, ±10% for all power range
Overall Efficiency	Higher than 90% for a 1.0 kW resistive load.
THD	< 5%
Manufacturing Cost	< $ 200
Packaging Volume	Less than 7.5 liters
Complete Packaging Weight	Less than 3 kg
Grid Connectivity	Must deliver energy into a grid with automatic detection at unity power factor. The unit should maintain the connection with grid when grid voltage and frequency varied within a certain of range. The unit must disconnect automatically from the utility grid and keep a standalone emergency load (maximum 250 W) if an external blackout or abnormal operating conditions occur with the grid.

Fig. 18. Power-stage hardware of the inverter prototype and blown-out view of the final package.

in Fig. 14(b) [17]. The design of the LCL filter follows the same procedure as described for the standalone inverter.

IV. CONTROL SCHEMES FOR THE STANDALONE AND THE GRID-CONNECTED MODES

The closed-loop controller operates in two modes: standalone and grid-connected. An SPDT relay is used to switch between the two modes of operation. The block diagrams of the inverter for the two modes are shown in Fig. 15. The power stage of the standalone inverter is shown in Fig. 3. For the grid-connected operation, an additional inductor is connected to the standalone inverter to reduce the distortion in the current injected into the utility grid.

For standalone operation of the inverter, we use a voltage-mode controller, as shown in Fig. 16. The controller is implemented on a digital platform using a TI TMS320C28X digital signal processor (DSP). To remove noise from the feedback signals, we use a second-order digital low-pass filter with a cutoff frequency of 500 Hz. The reference for the voltage is generated internally within the DSP. To ensure a regulated output voltage, a proportional–integral (PI) compensator is used. The input dc voltage is sensed to adapt the proportional gain of the PI compensator. A small integral gain is used to further filter the compensator output. As shown in Fig. 16, the rectified output of the compensator is sent to the UC3895 controller that is used to control the switches of the dc/ac converter by phase shifting the switching of one half-bridge of the converter with

TABLE III
LIST OF MAJOR COMPONENTS FOR POWER STAGE SHOWN IN FIG. 18

Designator	Manufacturer Part #	Specification
Q1-Q4	IRFP2907	N MOSFET 75 V, 209 A, $R_{ds(on)}$ 4.5 mΩ
S1-S4 & S1'-S4'	IRFPS40N50L	N MOSFET 500V, 40 A, $R_{ds(on)}$ 100 mΩ
Transformers T1, T2	Ferroxcube # TX74/39/13	14T: 91T, 20 kHz. With 0.65 µH leakage
Lf1	Magnetics. # 58868-A2	180 T, AWG # 14, 0.905 mH
Cf1	EPCOS # B81130C1225M	2.2 UF 275 V AC
Heat Sink # 1	Aavid Thermalloy # 78205	1.18"x 2.24"x 3.0"

respect to the other. It also allows a constant-frequency PWM and facilitates ZVS. The ac/ac converter switches primarily at line frequency (50 Hz/60 Hz) to minimize the switching losses.

The strategy for grid connection is shown in Fig. 17. When the grid-connection command is initiated, the grid voltage is used as the reference for the voltage-mode controller shown in Fig. 17(a). Compensation for any phase offset introduced due to the filters in the controller is ensured. The output of the inverter is synchronized (in amplitude, phase, and frequency) to the grid voltage. When synchronization is achieved, a relay between the inverter and the grid is operated near the zero crossing of the grid voltage to ensure that the inrush current into the inverter from the grid is minimized. Once the inverter is connected to the grid, a current-injection controller, as shown in Fig. 17(b), is activated. The rest of the controller is the same as that of the standalone controller described earlier.
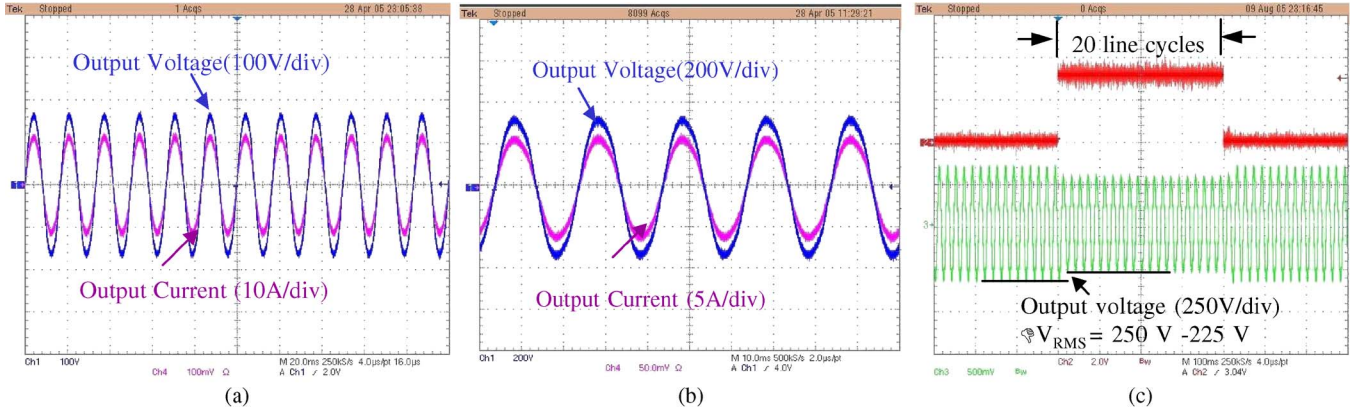
Fig. 19.   Experimental waveforms for standalone mode of operation. (a) 120-V/60-Hz and (b) 240-V/50-Hz steady-state outputs at 1000 W with an input voltage of 30 V. (c) Transient output voltage when the load changes from 250 to 3000 W and vice versa at 240 V/50 Hz. A relay is used to switch between two different load conditions, and the trigger signal for the relay is shown in the top trace.

V. PROTOTYPE AND EXPERIMENTAL RESULTS

The experimental prototype for the 1-kW grid-connected fuel-cell inverter was developed as part of the 2005 IEEE International Future Energy Challenge (FEC) competition. Table II shows some key design requirements. The major challenge was to design a compact and light-weight inverter, which can achieve more than 90% energy-conversion efficiency for a wide range of working conditions: 1) 250–1000-W load; 2) 30–60-V dc input; and 3) 120-V/60-Hz and 240-V/50-Hz ac outputs. The 1-kW experimental inverter prototype is shown in Fig. 18. An added challenge of designing the inverter for a cost target of < $ 200 was met, and the detailed bill of material was submitted by the University of Illinois team as a part of their final report for the IEEE FEC competition.

Major power-stage components are listed in Table III. Aluminum cabinet was found to be the best suited from the view points of weight and strength of the inverter package. For the top and the side walls of the cabinet, a 3-mm aluminum sheet was used, while for the bottom, a 4-mm aluminum sheet was used. The bottom sheet was reinforced in order to bear the weight of the inverter. The input/output electrical terminals were located at the rear of the inverter, while the keypad, the LCD display, the fan, and the parallel port for programming the DSP starter kit were located at the front. All of the magnetic components were clamped to the base of the cabinet, which also removed heat from the windings. The perforated windows and the fan were strategically placed to maximize the airflow for removing heat from the power semiconductors and the magnetic components.

Experimental results of the inverter prototype in the standalone mode of operation are shown in Fig. 19. The overall efficiency and THD of the fabricated inverter prototype, over the entire range of the load, are shown in Fig. 20. These data were measured using a Yokogawa power analyzer (model WT230).

The experimental results for the inverter prototype in the grid-connected mode are shown in Fig. 21. Fig. 21(c) shows the transient waveforms when the inverter is connected to the grid. Before connecting the inverter to the grid, the controller synchronizes the output of the inverter to the grid while continuing to support a standalone load. The relay for connecting the inverter to the grid is activated near the zero-crossing point

of the grid to reduce the inrush current. Fig. 21(d) shows the transient waveforms when the inverter is disconnected from the grid and connected to a standalone load.

VI. CONCLUSION

This paper has outlined the design issues of an isolated fuel-cell grid-connected inverter. It comprises a phase-shifted high-frequency dc/ac converter followed by a combination of two high-frequency transformers each with nominal primary-to-secondary turns ratio (N) of 6.5 and two ac/ac converters (whose outputs can be connected in parallel or series configuration for 120-V/60-Hz and 240-V/50-Hz ac outputs) for optimum solution of the universal power conditioner. The isolated-inverter approach achieves direct power conversion and does not require any intermediate filter components. Furthermore, the ac/ac converter is primarily line-switched, thereby practically mitigating the switching losses. In addition, the leakage of the high-frequency transformer is used to facilitate the ZVS of the dc/ac converter switches, thereby further reducing the switching losses. However, finite leakage inductance of the transformer leads to voltage spike at the secondary and loss in the duty ratio. Hence, an optimal design of the transformer, including cost consideration, is needed to achieve a tradeoff between ZVS of the dc/ac converter and the conduction loss of the ac/ac converter. On a related note, an adaptive transformer tapping was incorporated (which changes N from 6.5 to 4.3) to counter the impact of input-voltage variations on the inverter efficiency.

For the grid connection, the design of the output filter is critical. The output filters of the inverter are selected in such a manner so that they filter out the high-frequency components at the output of the ac/ac converter and generate a sinusoidal voltage and current, which satisfies the THD requirements. To reduce the inrush current during grid connection of the inverter, the digital controller of the inverter ensures that current injection is initiated when there is a close match between the phase, frequency, and amplitude of the grid and the inverter output voltages, and the grid voltage passes through a zero crossing. Moreover, the digital controller for the grid-connected inverter has been implemented to address the relatively slow transition time ($\sim$8 ms) of the relay.
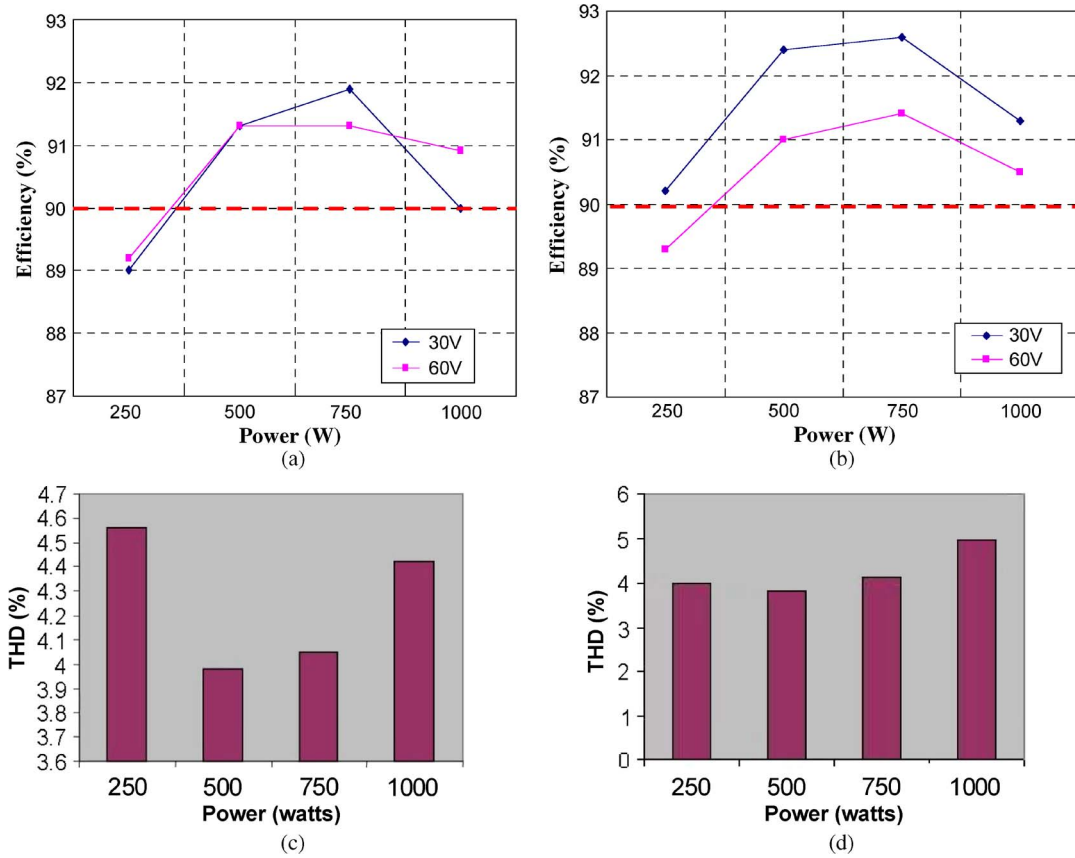
Fig. 20.   Experimentally measured efficiency and THD of the output voltage of the inverter. It is noted that $\pm 1\%$ variation in efficiency is possible. (a) 120-V/60-Hz and (b) 240-V/50-Hz ac outputs at 30- and 60-V inputs. THD results for (c) 120-V/60-Hz and (d) 240-V/50-Hz ac outputs.
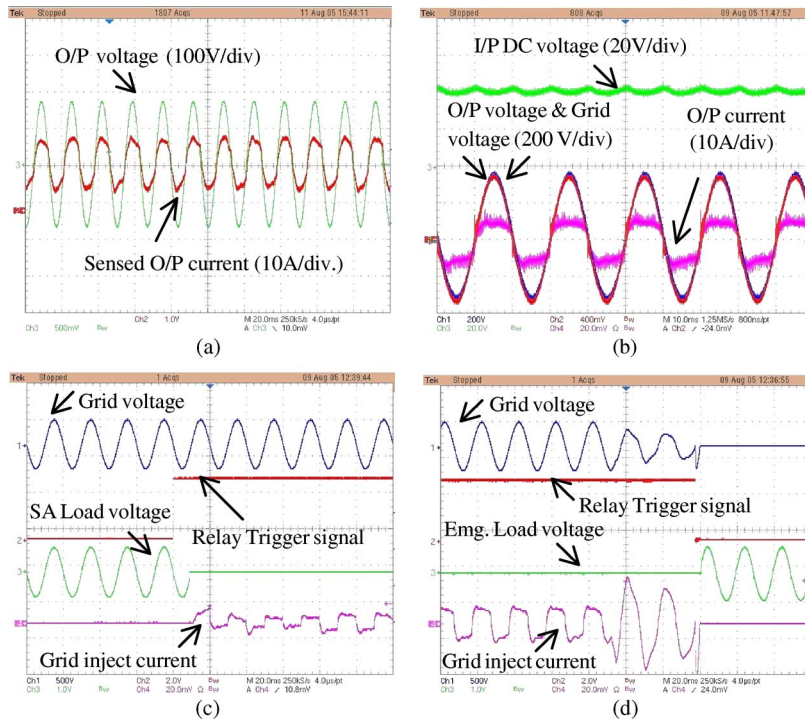

Fig. 21.   Experimental waveforms for the grid-connected mode of operation. (a) 120-V/60-Hz and (b) 240-V/50-Hz steady-state outputs at 1000 W with an input voltage of 40 V. (c) Transient waveforms when the inverter is connected to the grid. (d) Transient waveforms when the inverter is disconnected from the grid. *The distortion in the grid current is primarily due to the unavailability of a stiff grid or grid simulator in our laboratory at the time of experimentation. In the actual IEEE FEC competition held at the advanced facilities of the U.S. National Renewable Energy Laboratory (Colorado), no such distortions were observed, and the inverter met all design specifications and was adjudged the third best prototype in worldwide competition.*

Methodologies for further improvements in the overall energy-conversion efficiency of the inverter while simultaneously operating at higher switching frequency (for enhanced power density), using advanced semiconductor switches and soft-switching techniques, are being investigated. Extending the operation of the single-phase inverter for photovoltaic and battery-based sources as well as for higher power multiphase operation has added foci of our current research and development.

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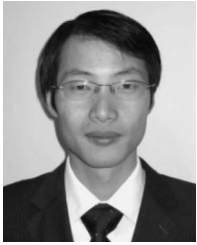
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A Universal Grid-Connected Fuel-Cell Inverter for Residential Application

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Muhammad Tahir, *Member, IEEE*, and Kaustuva Acharya, *Member, IEEE*

Abstract—This paper describes a universal fuel-cell-based grid-connected inverter design with digital-signal-processor-based digital control. The inverter has a direct power conversion mechanism with a high-frequency zero-voltage-switched dc/ac primary-side converter followed by a pair of ac/ac cycloconverters that operates either in parallel or in series to simultaneously address the issues of universal output and high efficiency. The critical design issues focus on the impact and optimization of transformer leakage inductance with regard to effectiveness of zero voltage switching of a primary-side converter, duty-cycle loss, resonance, and voltage spike that has effect on the breakdown voltage rating of the cycloconverter devices. An additional concept of dynamic transformer tapping has been explored to address the impact of varying input voltage on secondary-side voltage spike and inverter efficiency. Finally, detailed grid-parallel and grid-connected results are presented that demonstrate satisfactory inverter performances.

Index Terms—AC/AC, control, dc/ac, digital signal processor (DSP), fuel cell, grid, high frequency, inverter, residential.

I. INTRODUCTION

THE utilization of fuel cells for distributed power generation requires the development of a low-cost, high-efficiency, and universal power-electronic system that converts a fuel cell's low-voltage output, which usually varies from 30 to 60 V for residential application, into commercial 120-V/60-Hz and 240-V/50-Hz ac outputs [1]–[3]. In addition, the power-electronic system should have the following characteristics: 1) output-voltage regulation for a wide variation in the output voltage of the fuel-cell stack; 2) capability for standalone and grid-connected operations; 3) low output harmonics; and 4) high energy-conversion efficiency.

Fig. 1. Power-conditioning scheme with (a) line-frequency transformer, (b) high-frequency transformer in the dc/ac stage [7], (c) high-frequency transformer in the dc/dc stage [18], [19], and (d) single-stage isolated dc/ac converter [20].

Fig. 1(a)–(c) shows three mechanisms for achieving galvanic isolation between the fuel-cell stack and the application load. The conventional scheme, shown in Fig. 1(a), achieves isolation by placing a 50-Hz/60-Hz line-frequency transformer at the output of the inverter. Such a transformer is bulky because it has to handle low-frequency currents and voltages. The other two options, shown in Fig. 1(b) and (c), achieve isolation by placing the transformer within the power-conditioning system. The high-frequency isolation can be included in the dc/ac converter stage, as shown in Fig. 1(b) [7], or in the dc/dc converter stage, as shown in Fig. 1(c) [18], [19]. Fig. 1(d) shows an even more compact power-electronics option [20]. The single-stage isolated topology requires either a higher fuel-cell-stack

Fig. 2. Block diagram of high-frequency link inverter configurations: (a) dc/dc-type and (b) cycloconverter-type converter configurations.

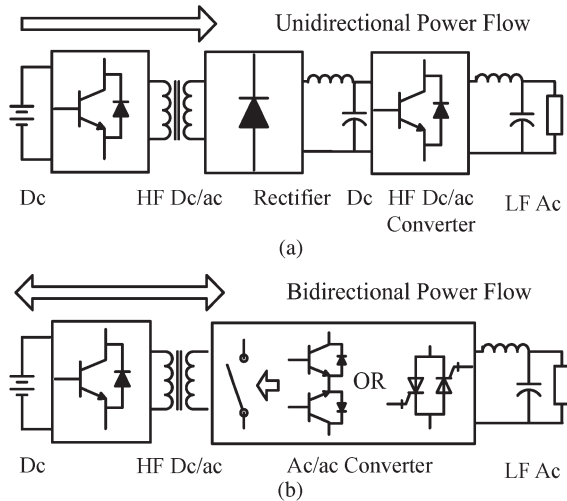voltage or slightly higher turns ratio of the transformer for a lower stack voltage to generate the needed 120-V/240-V line output. Overall, the isolation transformers for the schemes shown in Fig. 1(b)–(d) operate at high frequency and, hence, are significantly smaller than the line-frequency transformer shown in Fig. 1(a).

With regard to an isolated inverter, several topological configurations have been proposed to achieve fuel-cell power conversion at high efficiency without incurring high cost [1]–[10]. Based on where the transformer is inserted for isolating the stack from the load, these topologies can be broadly classified into two categories. The first one is referred to as the *"dc/dc-type converter"* and is shown in Fig. 2(a). It comprises a high-frequency dc/ac converter followed by a high-frequency transformer, a diode rectifier (inserted at the secondary of the transformer), and a link filter to obtain a higher dc voltage. Following this isolated dc/dc stage, a dc/ac converter is inserted to obtain a low-frequency ac. Because this type of topology has three power-conversion stages, it may not always be a suitable choice from efficiency and cost point of views because each of the power stages has to have very high efficiency. Furthermore, with increasing output power, the size and the cost of the dc-link filter attain significance.

The second topology, outlined in this paper and referred to as the *"cycloconverter-type converter,"* is shown in Fig. 2(b). This architecture supports bidirectional power flow and reduces system complexity by removing the rectifier and the dc-link filter. Galvanic isolation is achieved by embedding the transformer into the overall inverter, which usually comprises a two-level or higher level dc/ac converter followed by an ac/ac converter [1], [7], [8], [16].

Fig. 3 shows a circuit diagram of the proposed universal inverter with input voltage varying between 30 and 60 V. It comprises a phase-shifted full-bridge dc/ac converter as a common primary stage followed by two identical high-frequency step-up transformers and two forced ac/ac converters. Switches $Q_1 - Q_4$ of the dc/ac converter are sinusoidally modulated to create a high-frequency ac voltage, which is converted into a 60-Hz/50-Hz line-frequency ac by a combination of the ac/ac

converters and the LC output filters. As shown in Fig. 3(a) and (b), for 120- and 240-V ac outputs, the two filter capacitors of the ac/ac converters are connected in parallel and in series, respectively.

Phase-shifted control of the dc/ac converter enables $Q_1 - Q_4$ to be turned on under a zero-voltage-switching (ZVS) condition due to the resonance between the primary-side leakage inductance of the high-frequency transformer and the output capacitances of the MOSFETs [11]. Unlike the complex schemes outlined in the literature [9], [10], [12], which implement high-frequency switching for both the dc/ac converter and the ac/ac converter stages, the ac/ac converter switches in the control scheme outlined in this paper (see Figs. 16 and 17) are commutated primarily at line frequency when the polarities of output current and output voltage are the same and at high frequency when the polarities are opposite. Thus, under unity-power-factor operation, due to line-frequency switching, the ac/ac converter switching losses are significantly reduced.

Furthermore, unlike the topology outlined in [9] and [10], for an uninterruptible-power-supply application that usually has a high input voltage, in a fuel-cell-inverter application, owing to the low stack voltage, a step-up transformer with high turns ratio is necessary to obtain the rated ac output. For instance, for an input of 30 V, the primary-to-secondary turns ratio (N) of the transformer is calculated to be 13 to achieve the desired 240-V ac output. Fabrication of a 1-kW 1:13 high-frequency transformer is relatively difficult. Furthermore, high turns ratio yields enhanced secondary leakage inductance and secondary winding resistance, both of which result in a measurable loss in duty cycle and an increase in secondary copper loss. Higher leakage inductance also leads to higher voltage spike, which adds to the high nominal voltage of the secondary and necessitates the use of high-voltage power devices for the ac/ac converter. Such devices usually have higher on resistance and slower switching speeds, both of which diminish the overall system efficiency.

This paper addresses key design issues related to these challenges and proposes simple but effective solutions to improve efficiency. The focus of the design issues is on the effects of transformer leakage inductance on the ZVS and loss in the duty cycle of the dc/ac converter and on resonance, which results in voltage spike that affects the breakdown-voltage rating of the ac/ac converter devices. The concept of dynamic transformer tapping has been investigated to address the effects of input-voltage variation on voltage-spike mitigation and inverter efficiency. Subsequently, the control strategies for standalone and grid-connected operations and experimental design of a 1-kW inverter prototype are described. The experimental results and performances verify the effectiveness of the inverter and show its promising applications for fuel-cell as well as photovoltaic and battery-based power systems.

II. PRINCIPLES OF OPERATION

The basic schematic of the proposed universal inverter is shown in Fig. 4(a) and is used in the following sections to simplify the analysis. The ac/ac converters are switched based on output-voltage polarity, since primarily, unity-power-factor
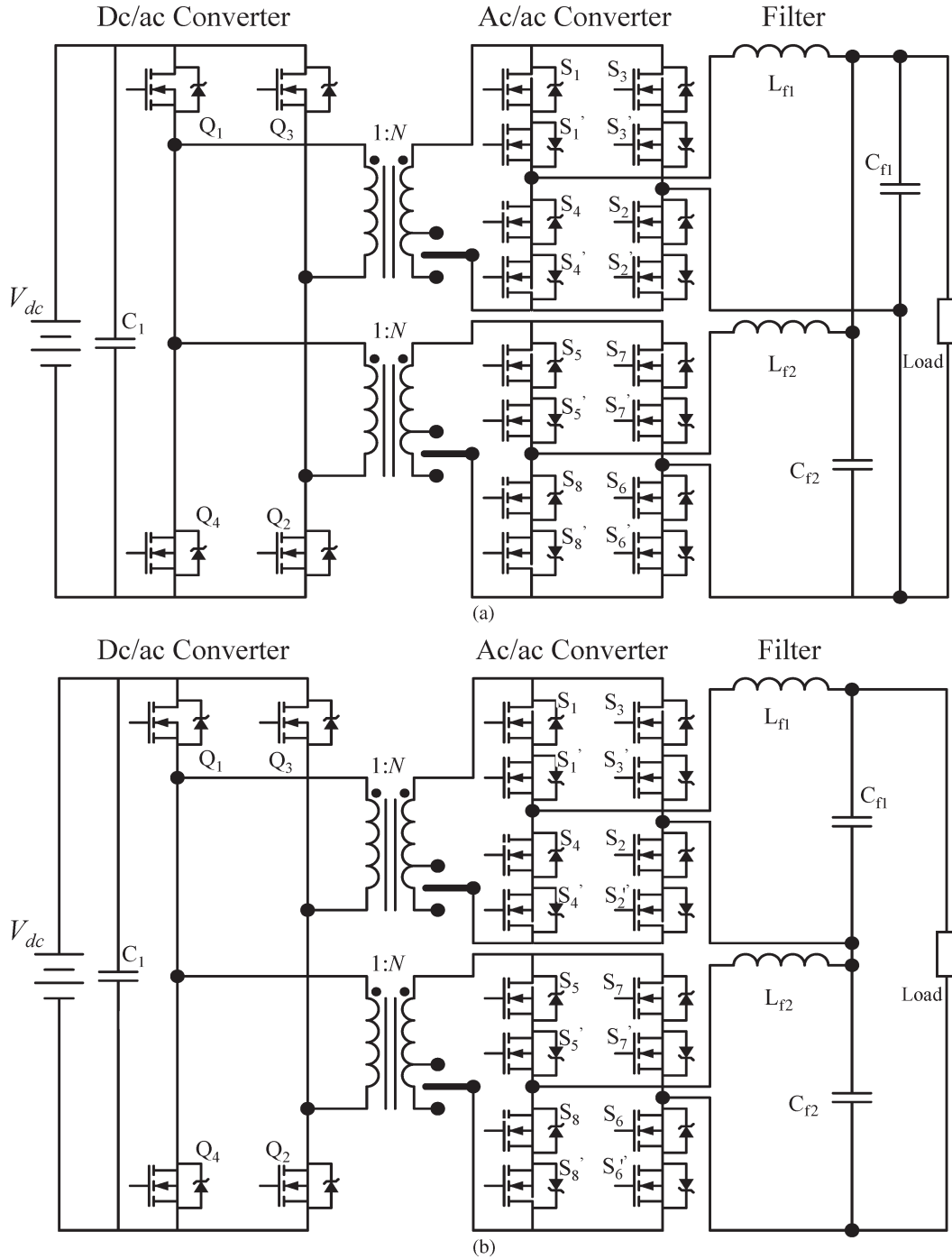
Fig. 3. Circuit diagrams of the proposed fuel-cell inverter for (a) 120-V/60-Hz ac and (b) 240-V/50-Hz ac outputs. An SPDT switch enables adaptive tapping of the transformer.

operation is required for the present design, and hence, the duration for which the polarities of the output voltage and current are different is negligibly small. The circuit schematic is the same as a conventional transformer-isolated full-bridge pulsewidth-modulation (PWM)-based dc/dc converter but has two different sets of rectifier arrangements for the positive and negative line cycles, as shown in Fig. 4(b) and (c). An illustration of the inverter operation is shown in Fig. 4(d), taking into account the two secondary-side ac/ac converters. Basically, the primary-side dc/ac converter is modulated to create a bipolar high-frequency waveform, which is amplified by the transformer and eventually shaped by the secondary-side ac/ac converters to generate the desired output ac waveform after passing the sinewave-modulated high-frequency signals through the output LC filter. Because the dc/ac converter creates the sinewave-modulated output, the ac/ac converter switches do not need to force switch; they can simply operate at line frequency to rectify the bipolar sinewave-modulated output. In practice, to preclude the reverse-recovery problem of the MOSFET, antiparallel diode, use of Schottky diode [21] or channel conduction of one of the MOSFETs [as shown in Fig. 4(d)] may need to be adopted.
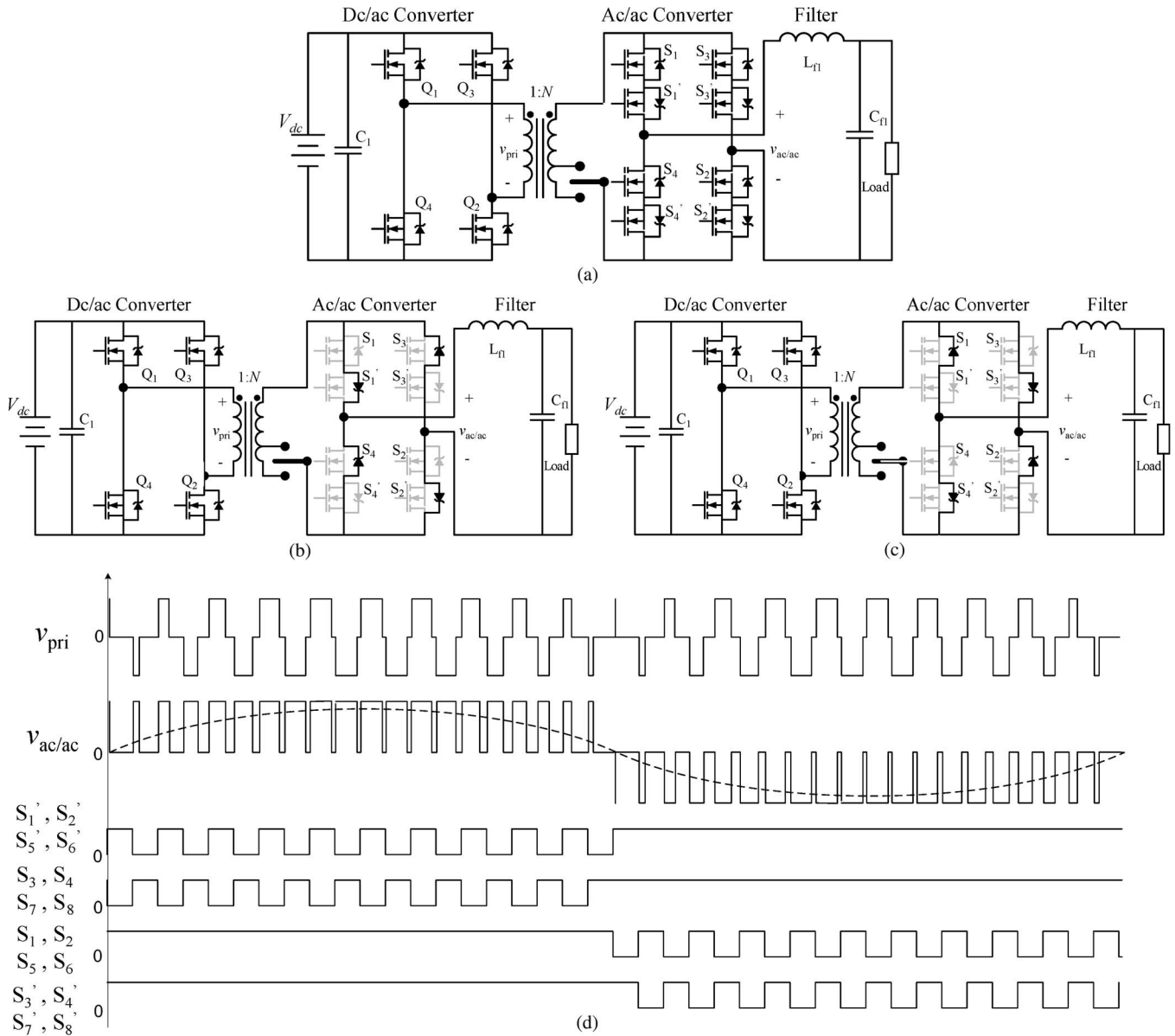
Fig. 4.   (a) Circuit elements of the inverter. Power-stage circuits for (b) positive and (c) negative line cycles. (d) Gate-drive signals and key waveforms.

Next, we discuss the modes of operation for 120-V ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same. The rationale for a tapped transformer is provided in Section III-C. Fig. 5(f) shows the waveforms for the five operating modes of the dc/ac converter for positive primary and positive filter-inductor currents. Modes 2 and 4 show the ZVS turn-on mechanism for switches Q_4 and Q_3, respectively. Overall, the five modes of the inverter operation are discussed next for a positive primary current. A set of five modes exists for a negative primary current as well. A similar set of five modes of operation and corresponding circuit configurations for 240-V ac output is shown in Fig. 6 for input voltage above 42 V (corresponding to $N = 4.3$). Again, the mode of operation for input voltage below 42 V (corresponding to $N = 6.5$) remains the same.

Mode 1 [Fig. 5(a)]: During this mode, switches Q_1 and Q_2 of the dc/ac converter are on, and the transformer primary currents i_{pri1} and i_{pri2} are positive. The output current (i_{out}) splits equally between the two ac/ac converter modules. For the top ac/ac converter module, $i_{out}/2$ is positive and flows through the switches S_1 and S_1', the output filter L_{f1} and C_{f1}, switches S_2 and S_2', and the transformer secondary. Similarly, for the bottom ac/ac converter module, $i_{out}/2$ is positive and flows through the switches S_5 and S_5', the output filter L_{f2} and C_{f2}, switches S_6 and S_6', and the transformer secondary.

Mode 2 [Fig. 5(b)]: At the beginning of this interval, the gate voltage of Q_1 undergoes a high-to-low transition. As a result, the output capacitance of Q_1 begins to accumulate charge, while the output capacitance of Q_4 begins to discharge. Once the voltage across Q_4 goes to zero, it can

Fig. 5. Modes of operation for 120-V/60-Hz ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). (a)–(e) Topologies corresponding to the five operating modes of the inverter for positive primary and positive filter-inductor currents. (f) Schematic waveforms show the operating modes of the dc/ac converter when primary currents are positive. The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same.

Fig. 6.   Modes of operation for 240-V/50-Hz ac output for an input-voltage range of 42–60 V (corresponding to $N = 4.3$). (a)–(e) Topologies corresponding to the five operating modes of the inverter for positive primary and positive filter-inductor currents. (f) Schematic waveforms show the operating modes of the dc/ac converter when primary currents are positive. The modes of operation below 42 V (corresponding to $N = 6.5$) remain the same.
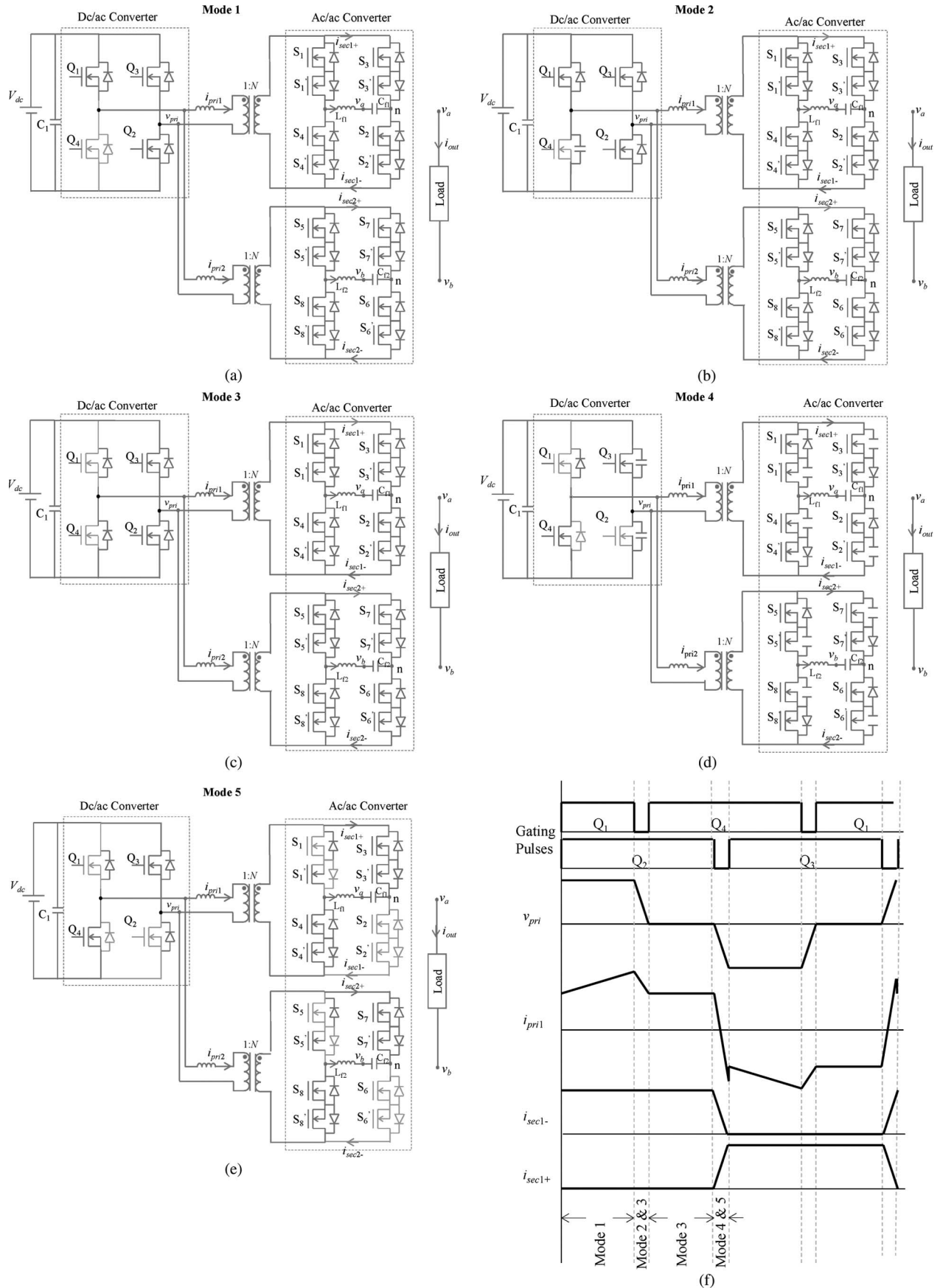
be turned on under ZVS. The transformer primary currents i_{pri1} and i_{pri2} and the load current i_{out} continue to flow in the same direction.

Mode 3 [Fig. 5(c)]: This mode initiates when Q_1 turns off. The transformer primary currents i_{pri1} and i_{pri2} are still positive and freewheel through Q_4 as shown in Fig. 5(c). Moreover, the load current continues to flow in the same direction as in Mode 2. Mode 3 ends when Q_2 starts to turn off.

Mode 4 [Fig. 5(d)]: At the beginning of this interval, the gate voltage of Q_2 undergoes a high-to-low transition. As a result, the output capacitance of Q_2 begins to accumulate charge, while the output capacitance of switch Q_3 begins to discharge, as shown in Fig. 5(d). The charging current of Q_2 and the discharging current of Q_3 together add up to the primary currents i_{pri1} and i_{pri2}. The transformer primary currents make a transition from positive to negative. Once the voltage across Q_3 goes to zero, it is turned on under ZVS condition. The load current flows in the same direction as in Mode 3 but makes a rapid transition from the bidirectional switches S_1 and S_1' and S_2 and S_2' to S_3 and S_3' and S_4 and S_4'. During this process, $i_{\text{out}}/2$ splits between the two legs each of the ac/ac converter modules as shown in Fig. 5(d). Mode 4 ends when the switch Q_2 is completely turned off and its output capacitance is charged to V_{dc}. At this point, it is necessary to note that, because S_1 and S_2 and S_5 and S_6 are off simultaneously, each of them supports a voltage of V_{dc}.

Mode 5 [Fig. 5(e)]: This mode starts when Q_2 is completely turned off. The primary currents i_{pri1} and i_{pri2} are negative, while the load current is positive as shown in Fig. 5(e).

Finally, and as shown in Fig. 4, there are always two MOSFET body diodes conducting current in each ac/ac converter, and the high-frequency ac voltage at the input of the ac/ac converter forces current commutation back and forth between one set of MOSFET diodes and the other. For instance, the MOSFET body diodes of the top ac/ac converter will switch alternately between S_1' and S_2' and S_3 and S_4 during the positive line cycle and between S_1 and S_2 and S_3' and S_4' during the negative line cycle. The enhanced efficiency of the ac/ac converter, realized due to line-frequency switching of the MOSFETs, is partially offset by the relatively higher forward-voltage drop and inefficient reverse-recovery characteristics of the MOSFET body diodes. External antiparallel diodes with lower voltage drop and faster reverse recovery will reduce the loss, thereby improving the efficiency.

The substitution of the MOSFET body-diode conduction by channel conduction of the MOSFET is another solution, which precludes the need for adding multiple external diodes in parallel. As shown in Fig. 4(d), the MOSFETs, which are previously turned on during a half-a-line cycle, will remain in the same state, while the MOSFETs previously in the off state will switch on and off to provide corresponding current paths along with their body diodes according to the polarity of high-frequency ac-link voltage. Majority of the current will flow through the lower resistance path of the MOSFET channels in the direction either from drain to source or from source to drain.
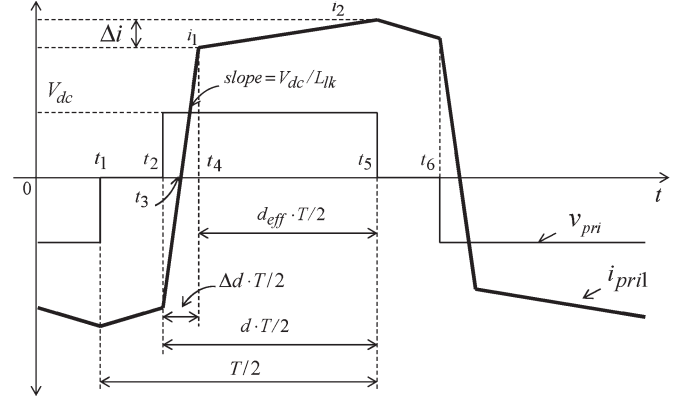

Fig. 7. Transformer primary-side voltage and current waveforms for the circuit shown in Fig. 3.

The body diodes of the MOSFETs will share a smaller amount of current. Compared with the body diode, the MOSFET channel usually has less on-state drop and enables faster switching speed. Consequently, the conduction and the switching losses will be relatively lower. However, synchronization of gate-drive signals between the dc/ac converter and the ac/ac converter switches is necessary in this case, which is realized by using the gate-drive signal of Q_1 and its complementary signal for controlling the ac/ac converter switches.

The switching pattern of the ac/ac converter, as shown in Fig. 4(d), was implemented, and its efficacy was verified via experimental tests on the inverter prototype. Approximately 1%–2% improvement in energy-conversion efficiency was obtained over the entire output power range by primarily enabling MOSFET-channel conduction instead of body-diode conduction.

III. DESIGN ISSUES

A. Duty-Ratio Loss

Fig. 7 shows one cycle of the primary-side high-frequency voltage and current waveforms for a conventional dc/dc converter [11]. Note that a significant difference between the operations of a dc/dc and a dc/ac converter is that the phase-shift angle of the former is controlled by a dc signal while it is modulated by a sinusoidal signal for the latter. The finite slope of the rising and falling edges of a transformer primary current due to the leakage inductance (L_{lk}), as shown in Fig. 7, will reduce the duty cycle (d). The duty-ratio loss is expressed as

$$\Delta d = \frac{i_1 + i_2}{\left(\frac{V_{\text{dc}}}{L_{lk}}\right) \cdot \left(\frac{T}{2}\right)} \tag{1}$$

where

$$i_1 = N \cdot (i_{\text{out}} - \Delta i/2) \tag{2}$$

$$i_2 = N \cdot \left(i_{\text{out}} + \Delta i/2 - \frac{v_{\text{out}}}{L_{f1}} \cdot (1 - d) \cdot T/2\right) \tag{3}$$

$$i_{\text{out}} = \frac{\sqrt{2}P_{\text{out}}}{v_{\text{out}}\cos(\phi)}. \tag{4}$$
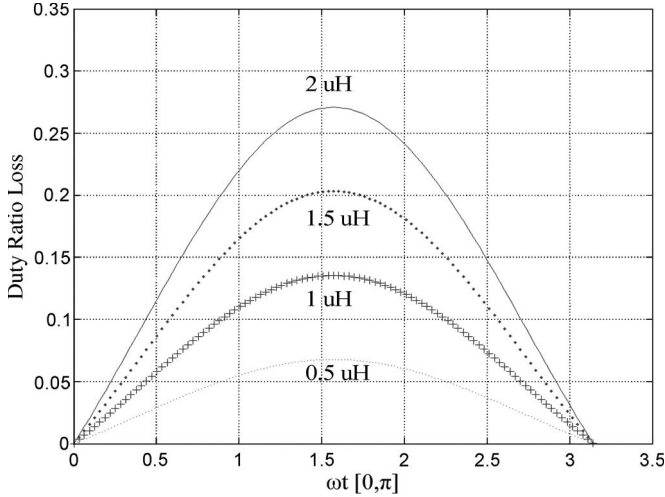
Fig. 8.   Variation of the duty-ratio loss as a function of the leakage inductance of the transformer over the half-a-line cycle.

TABLE I
CONDUCTING COMPONENTS AT DIFFERENT INTERVALS FOR THE CIRCUIT SHOWN IN FIG. 4(a). DIODES D_1-D_4 ARE ANTIPARALLEL DIODES OF Q_1-Q_4

Interval	Conducting Components
$t_1 \sim t_2$	D_1, Q_3
$t_2 \sim t_3$	D_1, D_2
$t_3 \sim t_4$	Q_1, Q_2
$t_4 \sim t_5$	Q_1, Q_2
$t_5 \sim t_6$	Q_2, D_4

In (2) and (3), N is the transformer turns ratio, L_{f1} is the output filter inductance, i_{out} is the filter current, v_{out} is the output voltage, T is the switching period, Δi is the filter inductor current ripple, P_{out} is the output power, and $\cos(\phi)$ is the load power factor. By substituting (2) and (3) into (1), we obtain

$$\Delta d = \frac{N}{\frac{V_{dc}}{L_{lk}} \cdot \frac{T}{2}} \cdot \left(2i_{out} - \frac{v_{out}}{L_{f1}} \cdot (1-d) \cdot \frac{T}{2} \right). \quad (5)$$

Unlike the dc/dc converter, the duty-ratio loss is time varying for the dc/ac converter due to the sinusoidal nature of v_{out}, i_{out}, and d. Assuming that L_{f1} is large enough, the second term within the parenthesis of (5) can be omitted. Thus, the duty-ratio loss has a sinusoidal shape and is proportional to N and L_{lk}. One can deduce from (5) that, due to the high turns ratio and low input voltage, even a small leakage inductance will cause a big duty-ratio loss.

Fig. 8 shows the calculated duty-ratio loss for a 1-kW inverter prototype for an input voltage of 30 V and for $N = 6.5$. Four parametric curves corresponding to four leakage inductances of 0.5, 1, 1.5, and 2 μH are shown. Fig. 8 shows that, for a leakage inductance of 2 μH, the duty-ratio loss is more than 25%. Consequently, a transformer with even higher turns ratio is required to compensate for this loss in the duty ratio, which increases the conduction loss and eventually decreases the efficiency as explained hereinafter.

The conducting components of the dc/ac converter during the half switching cycle (i.e., for duration $t_1 \sim t_6$) are listed in Table I. The equations to calculate conduction losses for the
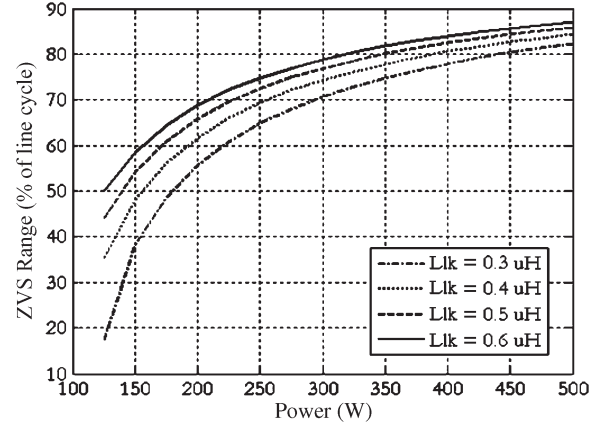

Fig. 9.   ZVS range of the dc/ac converter with variation in output power.

dc/ac converter switches can be simplified, provided that L_{f1} is large enough (i.e., i_1 equals i_2)

$$P_{Q1,4} = R_{on} \cdot \left(\left(\frac{i_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta d}{2} + i_1^2 \cdot d_{eff} \right) \quad (6)$$

$$P_{Q2,3} = R_{on} \cdot \left(\left(\frac{i_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta d}{2} + i_1^2 \cdot d_{eff} + i_1^2 \cdot (1-d) \right) \quad (7)$$

$$P_{D2,3} = \frac{i_1}{2} \cdot V_F \cdot \frac{\Delta d}{2} \quad (8)$$

$$P_{D1,4} = V_F \cdot \left(\frac{i_1}{2} \cdot \frac{\Delta d}{2} + i_1 \cdot (1-d) \right) \quad (9)$$

where V_F is the body-diode forward voltage drop of Q_1-Q_4, R_{on} represents their on resistances, and

$$d_{eff} = \frac{d}{\left(1 + 4 \frac{L_{lk}}{R_{load}} N^2 f_{SW} \right)}. \quad (10)$$

In (10), f_{SW} is the switching frequency of the dc/ac converter. From the aforementioned equations, it can be concluded that higher transformer leakage inductance yields lower value of effective duty ratio (d_{eff}). Therefore, to obtain the same output voltage, Δd [as described by (5)] increases to compensate for the reduction in d_{eff}, which results in a higher conduction loss. For the 1-kW inverter prototype under consideration, a combination of two transformers and two ac/ac converters on the secondary side of the high-frequency transformer is identified to be an optimum solution.

B. Optimization of the Transformer Leakage Inductance

The leakage inductance of the transformer aids in improving the ZVS range of the dc/ac converter but reduces the duty ratio of the converter that increases the conduction loss. Thus, the leakage inductance of each high-frequency transformer is designed to achieve the highest efficiency, as shown in Fig. 9.

For the sinusoidally modulated dc/ac converter, the ZVS capability is lost twice in every line cycle. The extent of the

loss of ZVS is a function of the output current. The available ZVS range (t_{ZVS}) as a percentage of the line cycle ($t_{\mathrm{LineCycle}}$) is given by

$$\frac{t_{\mathrm{ZVS}}}{t_{\mathrm{LineCycle}}} = \frac{2}{\pi}\sin^{-1}\left(\frac{1}{4}\frac{V_{\mathrm{dc}}^2\left(\frac{4}{3}C_{\mathrm{oss}}+\frac{1}{2}C_T\right)}{i_{\mathrm{out}}^2 L_{lk}}\right)^{\frac{1}{2}} \quad (11)$$

where C_{oss} is the device output capacitance and C_T is the interwinding capacitance of the transformer. When the dc/ac converter is not operating under ZVS condition, the devices are hard switched. In steady state, the switching loss (P_{SW}) of each MOSFET during hard switching depends on the switching frequency and the gate resistance (R_{GATE}) and is given by

$$P_{\mathrm{SW}} = \frac{V_{\mathrm{dc}}i_{\mathrm{out}}\sin(\omega t)}{2}f_{\mathrm{SW}}\left(t_{\mathrm{S(L\to H)}}+t_{\mathrm{S(H\to L)}}\right) \quad (12)$$

where ω is the line frequency in radians per second and the low-to-high and high-to-low transition times ($t_{\mathrm{S(L\to H)}}$ and $t_{\mathrm{S(H\to L)}}$) are given by

$$t_{\mathrm{S(L\to H)}} = \frac{Q_{\mathrm{G(SW)}}R_{\mathrm{GATE}}}{V_{\mathrm{DD}}-V_{\mathrm{SP}}} \quad t_{\mathrm{S(H\to L)}} = \frac{Q_{\mathrm{G(SW)}}R_{\mathrm{GATE}}}{V_{\mathrm{SP}}}. \quad (13)$$

In (13), $Q_{\mathrm{G(SW)}}$ is the gate charge, V_{DD} is the bias voltage of the gate driver, V_{SP} is the source voltage, and R_{GATE} is the gate resistance. The conduction loss of the MOSFET in steady state is described using

$$P_{\mathrm{cond1,3}} = R_{\mathrm{on}}\left[\left(\frac{i_1\sin(\omega t)}{\sqrt{3}}\right)^2\frac{\Delta d}{2}+i_{\mathrm{out}}^2\sin^2(\omega t)d_{\mathrm{eff}}\right] \quad (14)$$

$$P_{\mathrm{cond2,4}} = R_{\mathrm{on}}\left[\left(\frac{i_1\sin(\omega t)}{\sqrt{3}}\right)^2\frac{\Delta d}{2}+i_{\mathrm{out}}^2\sin^2(\omega t)d_{\mathrm{eff}}\right.$$

$$\left.+i_1^2\sin^2(\omega t)(1-d)\right]. \quad (15)$$

To optimize the leakage inductance, the total loss of the dc/ac converter over the half-a-line cycle has to be estimated, and it is determined using

$$P_{\mathrm{device}} = \frac{1}{\pi}\int_0^{\pi/\omega}\left(2P_{\mathrm{cond1,3}}+2P_{\mathrm{cond2,4}}+2P_{\mathrm{SW}}\frac{t_{\mathrm{ZVS}}}{t_{\mathrm{LineCycle}}}\right)\mathrm{d}t. \quad (16)$$

A numerical calculation of the total switching losses, as shown in Fig. 10, indicates that the optimal primary-side leakage inductance for the high-frequency transformer should be between 0.2 and 0.7 μH.

C. Transformer Tapping

The voltage variation on the secondary side of the high-frequency transformer necessitates high breakdown-voltage
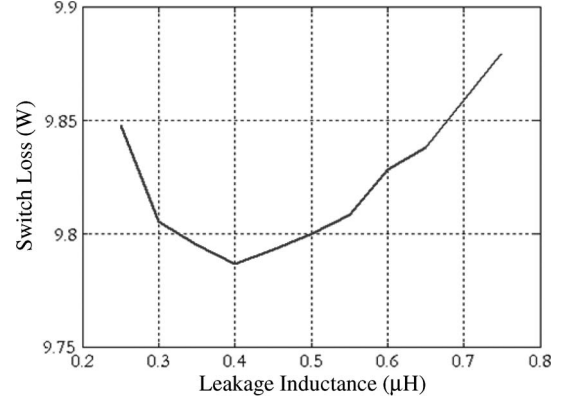

Fig. 10. Variation of the total switch loss of the dc/ac converter (for an output power of 500 W) with the leakage inductance of the high-frequency transformer. As the leakage inductance of the high-frequency transformer increases, the total switching loss decreases due to an increase in the range of ZVS, while the total conduction loss increases with increasing leakage inductance.
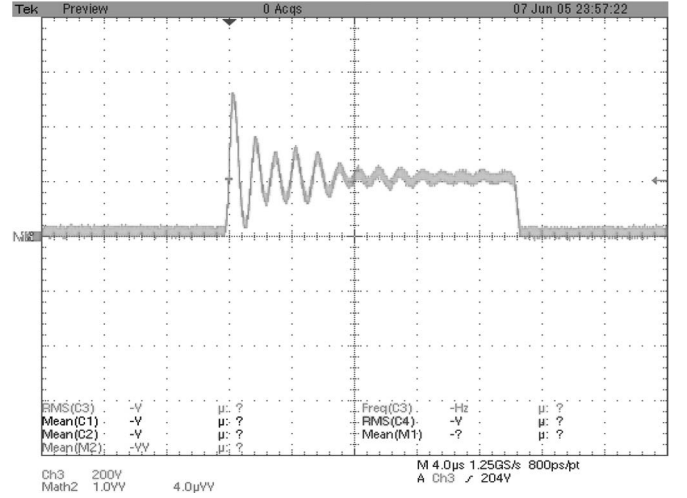

Fig. 11. Drain–source voltage across one of the ac/ac converter MOSFETs.

rating for the ac/ac converter switches and diminishes their utilization. For a step-up transformer with $N = 6.5$, the ac/ac converter switches have to withstand at least 390-V nominal voltage when input ramps to the high end (60 V), while only 195 V is required when 30 V is the input. In addition to the nominal voltage, the switches of the ac/ac converter have to tolerate the overshoot voltage (as shown in Fig. 11) caused by the oscillation between the leakage inductance of the transformer and the junction capacitances of the MOSFETs during turn-off [11]. The frequency of this oscillation is determined using

$$f_{\mathrm{ring}} = \frac{1}{2\pi\sqrt{N^2 L_{lk}C_{\mathrm{eq}}}} \quad (17)$$

where C_{eq} is the equivalent capacitance of the switch output capacitance and the parasitic capacitance of the transformer winding. The conventional passive snubber circuit or active-clamp circuits can be used to limit the overshoot, but they will induce losses and increase system complexity and component
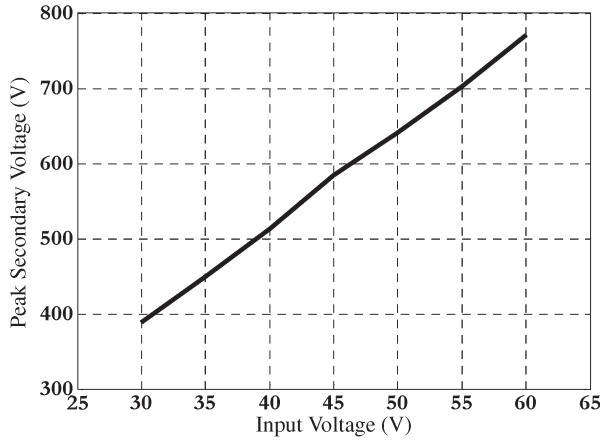
Fig. 12.   Peak voltage across the ac/ac converter with varying input voltage for a transformer primary leakage inductance of 0.7 μH, output capacitance of 240 pF (for the devices of the ac/ac converter), and output filter inductance and capacitance of 1 mH and 2.2 μF, respectively.
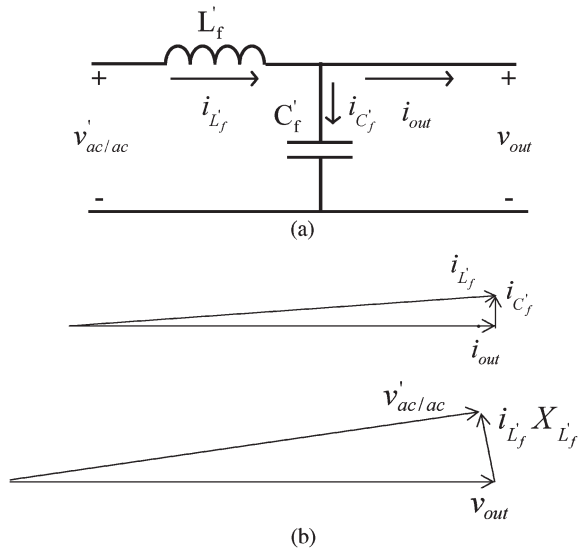

Fig. 13.   (a) Schematic of the LC filter for standalone operation of the fuel-cell inverter. (b) Phasor diagram describing the relationship among voltages and currents of the LC filter. Symbols $v'_{ac/ac}$, L'_f, and C'_f represent the equivalent output voltage of the ac/ac converter and the equivalent filter inductance and capacitance for 120- and 240-V ac output operations.

Fig. 14.   Two filter designs (along with their respective phasor diagrams) for the grid-connected inverter using (a) an L and (b) an LCL filter, connected between the inverter and the grid. Symbols $v'_{ac/ac}$, L'_f, and C'_f represent the equivalent output voltage of the ac/ac converter and the equivalent filter inductance and capacitance for 120- and 240-V ac output operations. Symbol L_{f3} represents the inductance between the grid and the inverter.

Fig. 15.   Schematics of the converters for (a) the standalone and (b) grid-connected modes of operation. An SPDT relay is used to switch between the two modes of operation.

costs. One simple but effective solution is to adjust the transformer turns ratio according to the input voltage.

To change the turns ratio of the high-frequency transformer, a bidirectional switch is required. Considering its simplicity and low conduction loss, a low-cost single-pole-double-throw (SPDT) relay is chosen for the inverter prototype, as shown in Fig. 3(a) and (b). For this prototype, for an input voltage in the range of 30–42 V, N equals 6.5. Hence, 500-V devices are used for the highest input voltage considering an 80% overshoot in the drain-to-source voltage that was observed in experiments. For an input voltage above 42 V, N equals 4.3, and hence, the same 500-V devices can still be used to cover the highest voltage as the magnitude of the voltage oscillation is reduced. The relay is activated near the zero-crossing point (where power transfer is negligible) to reduce the inrush current. Such an
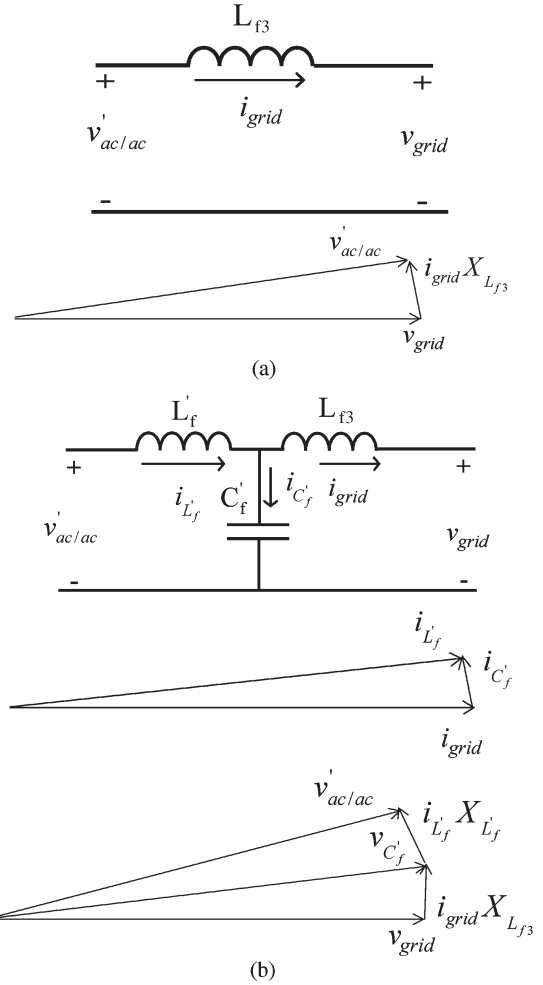
Fig. 16. Schematic of the voltage-mode controller for standalone operation of the inverter.

arrangement improves the efficiency of the transformer and significantly increases the utilization of the ac/ac converter switches for the full range of the input voltage. On the other hand, without adaptive transformer tapping, the minimal voltage rating for the devices is given by

$$V_{\mathrm{dc_{max}}} \cdot N \cdot (1 + 80\%) = 60 \cdot 6.5 \cdot 1.8 = 702 \text{ V}. \quad (18)$$

In practice, MOSFETs with 800 V or higher breakdown-voltage ratings are therefore required due to the lack of 700-V rating devices. The so-called rule of "silicon limit" (i.e., $R_{\mathrm{on}} \propto BV^{2.5}$, where BV is the breakdown voltage) indicates tha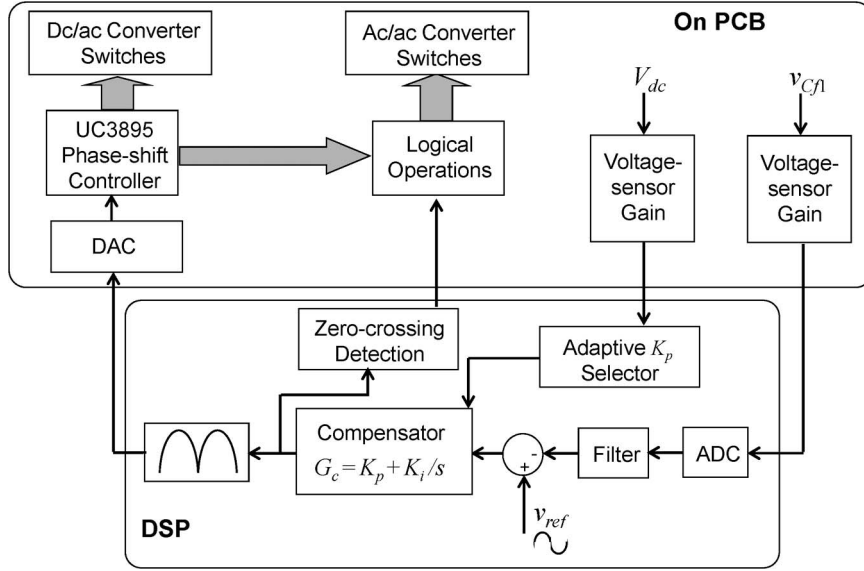t, in general, higher voltage rating MOSFETs will have higher R_{on} and hence higher conduction losses. It is noted that the exponent of BV can be different for other power semiconductor devices such as CoolMOS. Furthermore, for the same current rating, the switching speed of a MOSFET with higher breakdown voltage rating is usually slower. As such, if one uses a MOSFET with 800 V or higher voltage rating, converter efficiency is expected to degrade further due to enhanced power loss.

D. Effects of Resonance Between the Transformer Leakage Inductance and the Output Capacitance of the AC/AC Converter Switches

Resonance between the transformer leakage inductance and the output capacitance of the ac/ac converter devices causes the peak device voltage to exceed the nominal voltage (obtained in the absence of the transformer leakage inductance). This is shown in Fig. 12. Considering $N = 6.5$, one can observe that the peak secondary voltage can be around twice the nominal secondary voltage. Consequently, the breakdown-voltage rating of the ac/ac converter switches needs to be higher than the nominal value. As MOSFETs are used as switches, higher breakdown voltage entails increased on resistance that yields higher conduction loss. Thus, the *leakage*

affects the conduction loss and selection of the devices for the ac/ac converter.

The resonance begins only after the secondary current completes changing its direction and the ac/ac converter switches initiate turn-on or turn-off. During this resonance period, energy is transferred back and forth between the leakage and filter inductances and device and filter capacitances in an almost-lossless manner. The current through the switch, which supports the oscillating voltage, is almost zero. Thus, practically, no switching loss is incurred due to this resonance phenomenon, although it may have an impact on the electromagnetic-emission profile.

E. Output Filter Design for the Standalone and Grid-Connected Inverter

For the fuel-cell inverter, the design of the output filter is critical. The filter is so designed such that it mitigates the high-frequency components of the output of the ac/ac converter and generates a sinusoidal voltage and current that satisfies the total-harmonic-distortion (THD) requirements. For the standalone operation of the inverter, we choose a second-order filter whose phasor diagram is shown in Fig. 13. The value of the filter inductor is chosen to meet the current ripple requirement according to the IEEE 519 standard and is given by [13]

$$L'_f > \frac{1}{8} \frac{N V_{\mathrm{dc}}}{0.2 (i_{\mathrm{out}}) f_{\mathrm{SW}}}.$$

Fig. 13 shows that the current $(i_{C'_f})$ through C'_f increases the reactive power drawn from the converter, which has an adverse effect on the efficiency of the fuel-cell inverter. The current through the capacitor is given by $i_{C'_f} = v_{\mathrm{out}}/\omega C'_f$, which shows that, if the capacitance is high, the amount of reactive current drawn from the inverter increases. The capacitance design is a tradeoff between the THD requirements and the tolerable reactive power drawn by the system. To meet the
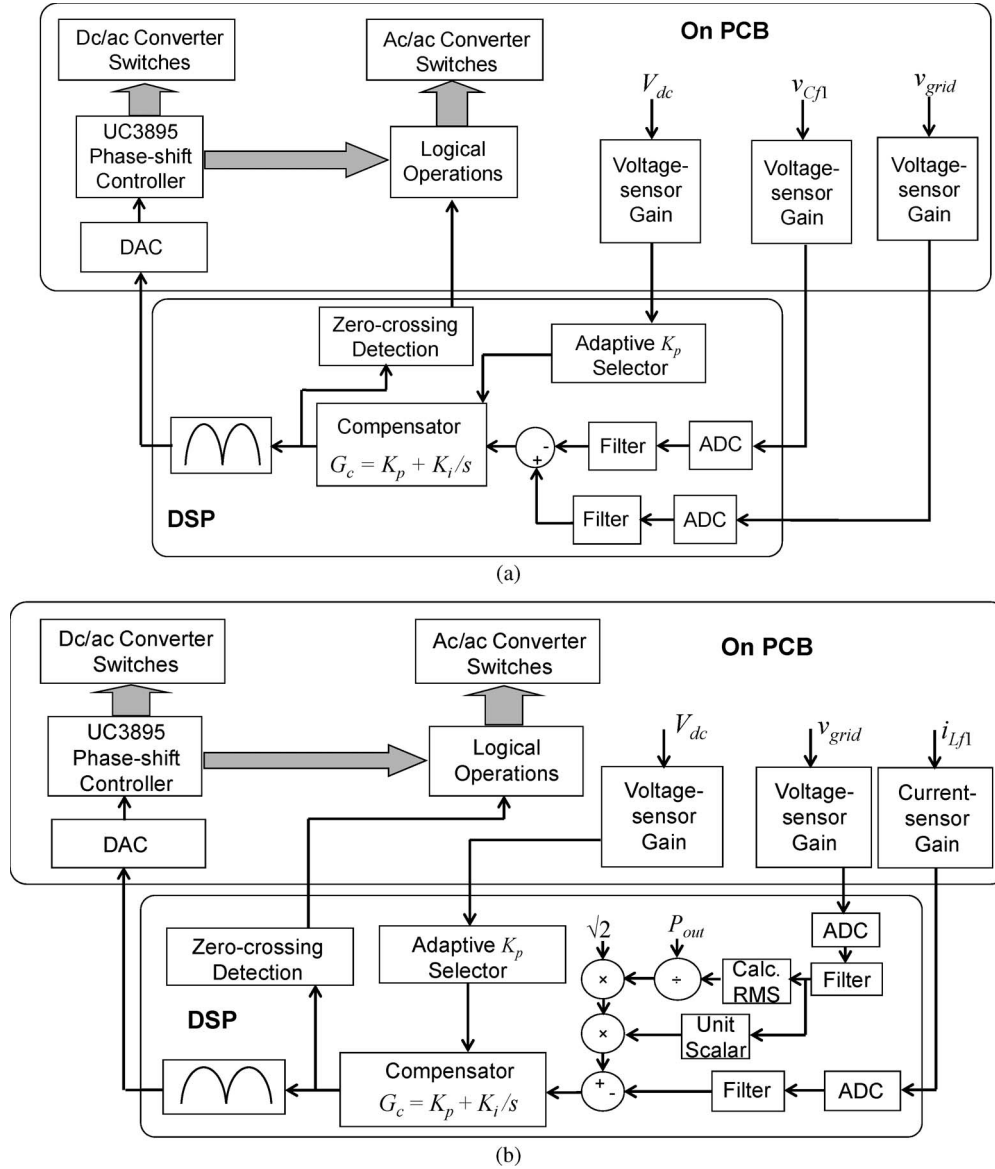
Fig. 17.   (a) Schematic of the voltage-mode controller for the standalone inverter just before grid connection. (b) Schematic of the current-injection controller for the inverter after it is connected to the grid.

requirements of the IEEE 519 standard, the value of the filter capacitance is chosen to be [13]

$$C_f' = (\%P_{\text{Reactive}}) \frac{P_{\text{outrated}}}{\omega v_{\text{out}}^2}$$

where $\%P_{\text{Reactive}}$ is the tolerable reactive power and P_{outrated} is the rated output power of the inverter.

For the grid-connected operation, the inverter should have an inductive output to minimize the inrush current between the grid and the inverter. In Fig. 14, we outline two possible choices: a single-inductor (L) and an inductive–capacitive–inductive (LCL) filter. In [14] and [15], a simple L filter is proposed for the grid connection. However, to meet the regulatory standards of IEEE 519 or IEC 61000-3-2, the size of such an inductor has to be significantly large. This is mainly because the inductor has to bypass the higher order harmonics of the ac/ac output. Hence, we choose an LCL filter, as shown

TABLE II
SOME KEY DESIGN SPECIFICATIONS FOR THE INVERTER [1], [2]

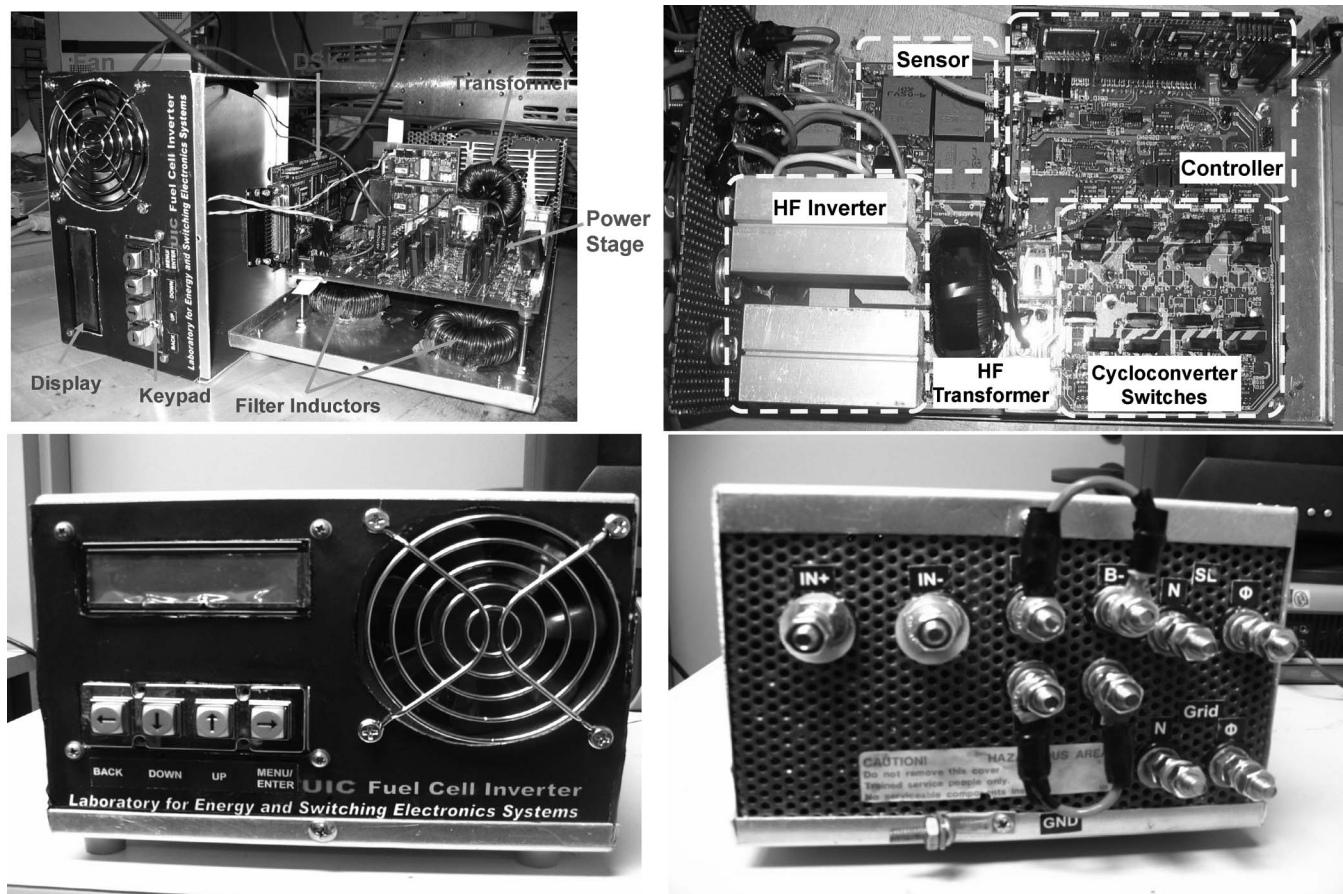|	
Input Source	30-60 V dc
Output Power	Up to 1 kW continuous, 3 kW for 20 line cycles
Output Voltage	120 V/60 Hz and 240 V/50 Hz ac outputs, ±10% for all power range
Overall Efficiency	Higher than 90% for a 1.0 kW resistive load.
THD	< 5%
Manufacturing Cost	< $ 200
Packaging Volume	Less than 7.5 liters
Complete Packaging Weight	Less than 3 kg
Grid Connectivity	Must deliver energy into a grid with automatic detection at unity power factor. The unit should maintain the connection with grid when grid voltage and frequency varied within a certain of range. The unit must disconnect automatically from the utility grid and keep a standalone emergency load (maximum 250 W) if an external blackout or abnormal operating conditions occur with the grid.

Fig. 18. Power-stage hardware of the inverter prototype and blown-out view of the final package.

in Fig. 14(b) [17]. The design of the LCL filter follows the same procedure as described for the standalone inverter.

IV. CONTROL SCHEMES FOR THE STANDALONE AND THE GRID-CONNECTED MODES

The closed-loop controller operates in two modes: standalone and grid-connected. An SPDT relay is used to switch between the two modes of operation. The block diagrams of the inverter for the two modes are shown in Fig. 15. The power stage of the standalone inverter is shown in Fig. 3. For the grid-connected operation, an additional inductor is connected to the standalone inverter to reduce the distortion in the current injected into the utility grid.

For standalone operation of the inverter, we use a voltage-mode controller, as shown in Fig. 16. The controller is implemented on a digital platform using a TI TMS320C28X digital signal processor (DSP). To remove noise from the feedback signals, we use a second-order digital low-pass filter with a cutoff frequency of 500 Hz. The reference for the voltage is generated internally within the DSP. To ensure a regulated output voltage, a proportional–integral (PI) compensator is used. The input dc voltage is sensed to adapt the proportional gain of the PI compensator. A small integral gain is used to further filter the compensator output. As shown in Fig. 16, the rectified output of the compensator is sent to the UC3895 controller that is used to control the switches of the dc/ac converter by phase shifting the switching of one half-bridge of the converter with

TABLE III
LIST OF MAJOR COMPONENTS FOR POWER STAGE SHOWN IN FIG. 18

Designator	Manufacturer Part #	Specification
Q1-Q4	IRFP2907	N MOSFET 75 V, 209 A, $R_{ds(on)}$ 4.5 mΩ
S1-S4 & S1'-S4'	IRFPS40N50L	N MOSFET 500V, 40 A, $R_{ds(on)}$ 100 mΩ
Transformers T1, T2	Ferroxcube # TX74/39/13	14T: 91T, 20 kHz. With 0.65 μH leakage
Lf1	Magnetics. # 58868-A2	180 T, AWG # 14, 0.905 mH
Cf1	EPCOS # B81130C1225M	2.2 UF 275 V AC
Heat Sink # 1	Aavid Thermalloy # 78205	1.18"x 2.24"x 3.0"

respect to the other. It also allows a constant-frequency PWM and facilitates ZVS. The ac/ac converter switches primarily at line frequency (50 Hz/60 Hz) to minimize the switching losses.

The strategy for grid connection is shown in Fig. 17. When the grid-connection command is initiated, the grid voltage is used as the reference for the voltage-mode controller shown in Fig. 17(a). Compensation for any phase offset introduced due to the filters in the controller is ensured. The output of the inverter is synchronized (in amplitude, phase, and frequency) to the grid voltage. When synchronization is achieved, a relay between the inverter and the grid is operated near the zero crossing of the grid voltage to ensure that the inrush current into the inverter from the grid is minimized. Once the inverter is connected to the grid, a current-injection controller, as shown in Fig. 17(b), is activated. The rest of the controller is the same as that of the standalone controller described earlier.
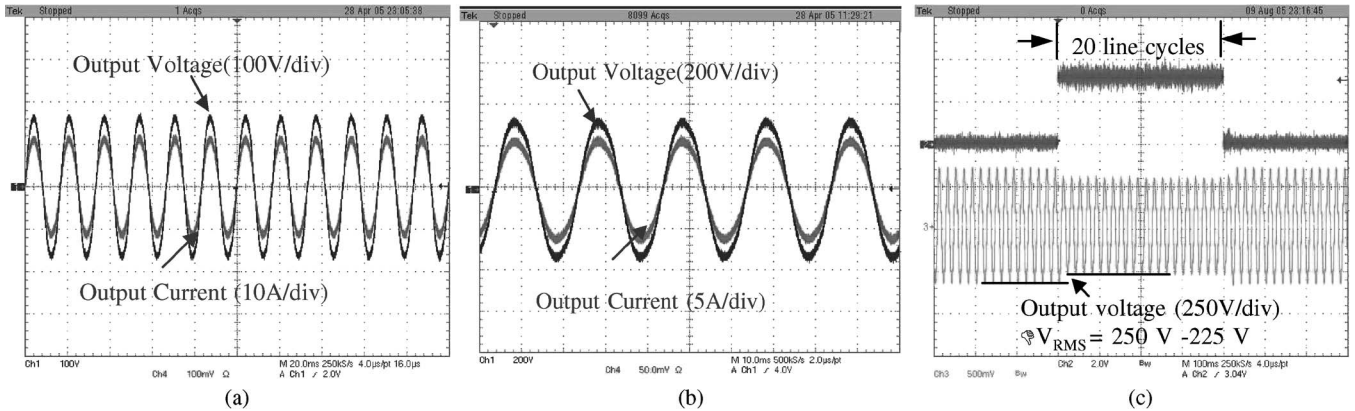
Fig. 19.   Experimental waveforms for standalone mode of operation. (a) 120-V/60-Hz and (b) 240-V/50-Hz steady-state outputs at 1000 W with an input voltage of 30 V. (c) Transient output voltage when the load changes from 250 to 3000 W and vice versa at 240 V/50 Hz. A relay is used to switch between two different load conditions, and the trigger signal for the relay is shown in the top trace.

V. PROTOTYPE AND EXPERIMENTAL RESULTS

The experimental prototype for the 1-kW grid-connected fuel-cell inverter was developed as part of the 2005 IEEE International Future Energy Challenge (FEC) competition. Table II shows some key design requirements. The major challenge was to design a compact and light-weight inverter, which can achieve more than 90% energy-conversion efficiency for a wide range of working conditions: 1) 250–1000-W load; 2) 30–60-V dc input; and 3) 120-V/60-Hz and 240-V/50-Hz ac outputs. The 1-kW experimental inverter prototype is shown in Fig. 18. An added challenge of designing the inverter for a cost target of < $ 200 was met, and the detailed bill of material was submitted by the University of Illinois team as a part of their final report for the IEEE FEC competition.

Major power-stage components are listed in Table III. Aluminum cabinet was found to be the best suited from the view points of weight and strength of the inverter package. For the top and the side walls of the cabinet, a 3-mm aluminum sheet was used, while for the bottom, a 4-mm aluminum sheet was used. The bottom sheet was reinforced in order to bear the weight of the inverter. The input/output electrical terminals were located at the rear of the inverter, while the keypad, the LCD display, the fan, and the parallel port for programming the DSP starter kit were located at the front. All of the magnetic components were clamped to the base of the cabinet, which also removed heat from the windings. The perforated windows and the fan were strategically placed to maximize the airflow for removing heat from the power semiconductors and the magnetic components.

Experimental results of the inverter prototype in the standalone mode of operation are shown in Fig. 19. The overall efficiency and THD of the fabricated inverter prototype, over the entire range of the load, are shown in Fig. 20. These data were measured using a Yokogawa power analyzer (model WT230).

The experimental results for the inverter prototype in the grid-connected mode are shown in Fig. 21. Fig. 21(c) shows the transient waveforms when the inverter is connected to the grid. Before connecting the inverter to the grid, the controller synchronizes the output of the inverter to the grid while continuing to support a standalone load. The relay for connecting the inverter to the grid is activated near the zero-crossing point

of the grid to reduce the inrush current. Fig. 21(d) shows the transient waveforms when the inverter is disconnected from the grid and connected to a standalone load.

VI. CONCLUSION

This paper has outlined the design issues of an isolated fuel-cell grid-connected inverter. It comprises a phase-shifted high-frequency dc/ac converter followed by a combination of two high-frequency transformers each with nominal primary-to-secondary turns ratio (N) of 6.5 and two ac/ac converters (whose outputs can be connected in parallel or series configuration for 120-V/60-Hz and 240-V/50-Hz ac outputs) for optimum solution of the universal power conditioner. The isolated-inverter approach achieves direct power conversion and does not require any intermediate filter components. Furthermore, the ac/ac converter is primarily line-switched, thereby practically mitigating the switching losses. In addition, the leakage of the high-frequency transformer is used to facilitate the ZVS of the dc/ac converter switches, thereby further reducing the switching losses. However, finite leakage inductance of the transformer leads to voltage spike at the secondary and loss in the duty ratio. Hence, an optimal design of the transformer, including cost consideration, is needed to achieve a tradeoff between ZVS of the dc/ac converter and the conduction loss of the ac/ac converter. On a related note, an adaptive transformer tapping was incorporated (which changes N from 6.5 to 4.3) to counter the impact of input-voltage variations on the inverter efficiency.

For the grid connection, the design of the output filter is critical. The output filters of the inverter are selected in such a manner so that they filter out the high-frequency components at the output of the ac/ac converter and generate a sinusoidal voltage and current, which satisfies the THD requirements. To reduce the inrush current during grid connection of the inverter, the digital controller of the inverter ensures that current injection is initiated when there is a close match between the phase, frequency, and amplitude of the grid and the inverter output voltages, and the grid voltage passes through a zero crossing. Moreover, the digital controller for the grid-connected inverter has been implemented to address the relatively slow transition time (∼8 ms) of the relay.
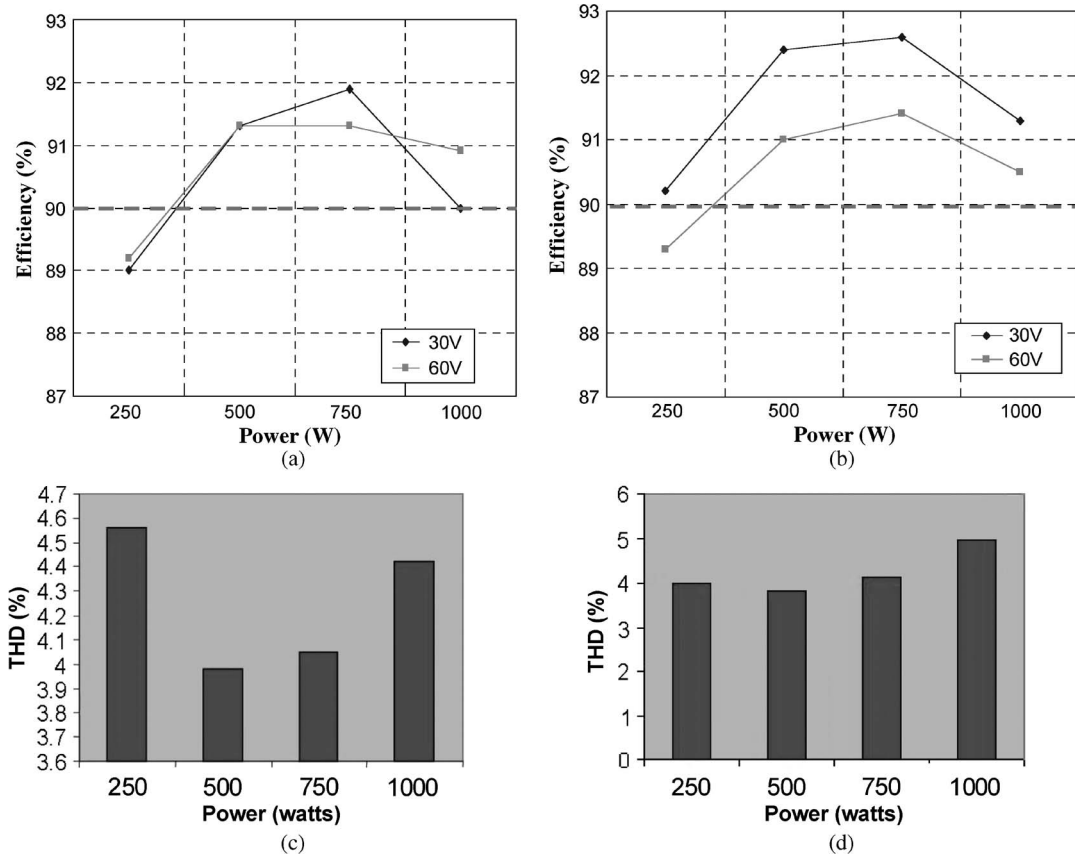
Fig. 20. Experimentally measured efficiency and THD of the output voltage of the inverter. It is noted that ±1% variation in efficiency is possible. (a) 120-V/60-Hz and (b) 240-V/50-Hz ac outputs at 30- and 60-V inputs. THD results for (c) 120-V/60-Hz and (d) 240-V/50-Hz ac outputs.
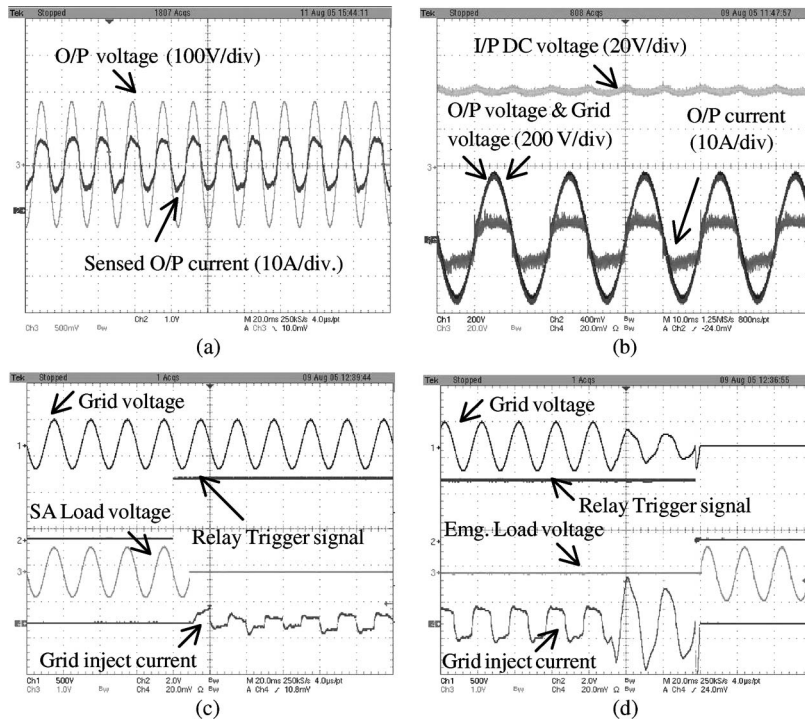

Fig. 21. Experimental waveforms for the grid-connected mode of operation. (a) 120-V/60-Hz and (b) 240-V/50-Hz steady-state outputs at 1000 W with an input voltage of 40 V. (c) Transient waveforms when the inverter is connected to the grid. (d) Transient waveforms when the inverter is disconnected from the grid. *The distortion in the grid current is primarily due to the unavailability of a stiff grid or grid simulator in our laboratory at the time of experimentation. In the actual IEEE FEC competition held at the advanced facilities of the U.S. National Renewable Energy Laboratory (Colorado), no such distortions were observed, and the inverter met all design specifications and was adjudged the third best prototype in worldwide competition.*

Methodologies for further improvements in the overall energy-conversion efficiency of the inverter while simultaneously operating at higher switching frequency (for enhanced power density), using advanced semiconductor switches and soft-switching techniques, are being investigated. Extending the operation of the single-phase inverter for photovoltaic and battery-based sources as well as for higher power multiphase operation has added foci of our current research and development.

ACKNOWLEDGMENT

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He is currently the Director of the Laboratory for Energy and Switching Electronics Systems, Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, where he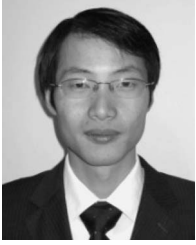 is also an Associate Professor. He is a Reviewer for multiple international journals and conferences. He was the Editor-in-Chief for the *International Journal of Power Management Electronics* between 2006 and 2009. He has over 15 years of professional experience and has held R&D and design positions in leading industrial organizations. He has published over 100 refereed and invited journals and conference papers. His current areas of interests are interactive power electronics/power networks, renewable and alternate energy systems, photonically triggered and wide-bandgap power semiconductor devices, and applied technologies.

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