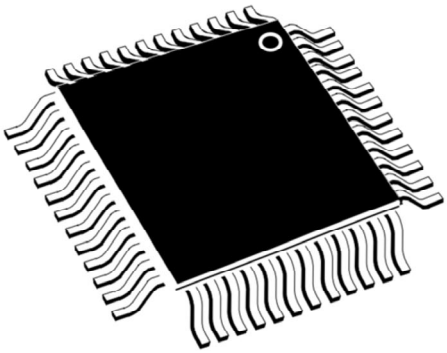
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.

Overview



- Provides interface for interaction with external environment
  - Fully configurable
  - With interrupt and wake-up capability
  - Direct connection to IOPORT from CPU

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to IOPORT allows fast toggle/sampling response

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General-purpose IO pins of STM32 microcontrollers provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals.
Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Differences with STM32F0

- The GPIO interfaces are similar to STM32F0 microcontrollers, with some small differences.

	STM32F0	STM32G0
Reset state	Input mode	Analog mode
Connection to cortex	AHB bus	IOPORT
Pull up/down in LP modes	No	Yes (Configured in PWR Controller)

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This table shows the differences with the STM32F0 microcontroller.
When STM32G0 microcontrollers are in reset state, most of the IO ports are configured in analog mode to minimize energy consumption.
The Cortex®-M0+ core has direct access to the GPIO registers through the single-cycle I/O port bus. This provides a low-latency direct path to change the state of outputs or to read the state of inputs.
The pull-up or pull-down resistors independently configured for any IO pin may remain active while entering a low-power mode. It is configured in the PWR module.

Key features

- Bi-directional operation of up to 60* I/O pins
  - Shared across up to 5 GPIO ports named GPIOA to GPIOF, with up to 16 I/O pins per port
    - All with external interrupt and wake-up capabilities
  - Atomic bit set and bit reset using BSRR and BRR registers
  - Independent configuration for each I/O pin
- GPIOx directly connected to IOPORT bus
- Most I/O pins are 5 V tolerant

* : depends on part numbers and packages

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General-purpose I/Os provide bidirectional operation – input and output – with an independent configuration for each I/O pin. They are shared across up to 5 ports named GPIOA to GPIOD, and GPIOF.
Each of them host up to 16 I/O pins. I/O ports support atomic bit set and reset operations through BSRR and BRR registers.
I/O ports are directly connected to the single-cycle IO port bus. This allows fast I/O pin operations, e.g. toggling of the pin every two clock cycles. No conflict with the DMA can occur because this Cortex®-M0+ port is private to the CPU.
Most of the I/O pins are 5 V tolerant when supplied from VDDIOx above 1.6 V.

Operating modes

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Flexible operating modes to best fit application needs

- Input mode
  - Floating (no pull resistor), input with pull-up/down, analog input mode
- Output mode
  - Push-pull, open drain with optional pull-up/down
- Configurable output slew rate speed up to 56 MHz
- Alternate function mode
- Locking mechanism to freeze the I/O port configuration (GPIOx_LCKR)

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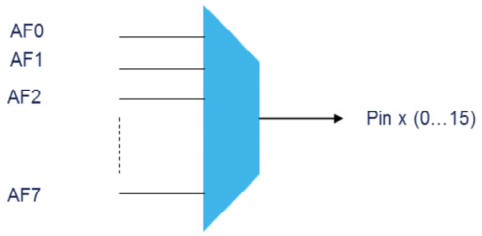
General-purpose I/O pins can be configured into several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges to ensure the best compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.
I/O pins are also used by other integrated peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
The configuration of the I/O ports can be locked to

increase application robustness. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as interface by other embedded peripherals

- Several integrated peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers (x = A..D, F)



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Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to the I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.

IO pin configuration

GPIOx_MODER[MODEi]	GPIOx_OTYPER[OTi]	GPIOx_PUPDR[PUPDi]	I/O configuration
0b00 (Input)		0b00 (No pull-up/pull_down)	Input, floating
		0b01 (Pull-up)	Input, pull-up
		0b10 (Pull-down)	Input, pull-down
0b01 (Output)	0 (Push-pull)	0b00 (No pull-up/pull_down)	GP output, push-pull, floating
		0b01 (Pull-up)	GP output, push-pull, pull-up
		0b10 (Pull-down)	GP output, push-pull, pull-down
	1 (Open-drain)	0b00 (No pull-up/pull_down)	GP output, open-drain, floating
		0b01 (Pull-up)	GP output, open-drain, pull-up
		0b10 (Pull-down)	GP output, open-drain, pull-down
0b10 (Alternate function)	0 (Push-pull)	0b00 (No pull-up/pull_down)	AF output, push-pull, floating
		0b01 (Pull-up)	AF output, push-pull, pull-up
		0b10 (Pull-down)	AF output, push-pull, pull-down
	1 (Open-drain)	0b00 (No pull-up/pull_down)	AF output, open-drain, floating
		0b01 (Pull-up)	AF output, open-drain, pull-up
		0b10 (Pull-down)	AF output, open-drain, pull-down
0b11 (Analog)	x	0bxx	Analog input

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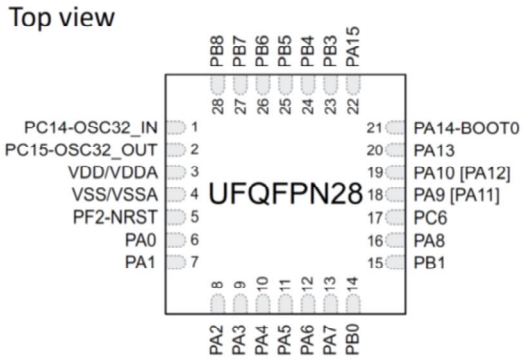
The configuration of any IO pin is achieved through 3 registers: GPIOx_MODER, GPIOx_OTYPER, GPIOx_PUPDR.

- Register GPIOx_MODER selects the functionality of the IO pin: digital input, digital output, digital alternate function or analog.
- Register GPIO_OTYPER is relevant when the pin is an output: it selects open drain vs push-pull operation.
- Register GPIOx_PUPDR is relevant when the pin is not configured in analog mode. It enables /disables pull-up and pull-down resistors.

Remapable GPIOs

- Two GPIOs PA12 and PA11 can be remapped by PA10 and PA9 respectively in order to give access to their functions when the pins are not natively available on the package.
  - The remap is handled through the SYS_CFG register



The two pins PA9 and PA10 can remap the two GPIOs PA11 and PA12 respectively in order to give access to their functions when the pins are not natively available on the package.
With this remapping, alternate functions related to pins PA9 and PA10 are available.
Note that this remapping also applies when the package supports pins PA9 and PA10 as independent pins.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default to analog mode
  - Saves current consumption during and after reset (Schmitt trigger is off)
- Only SWD debug pins remain in AF pull-up/pull-down configuration
  - PA13: SWDIO
  - PA14: SWCLK **(BOOT0)**

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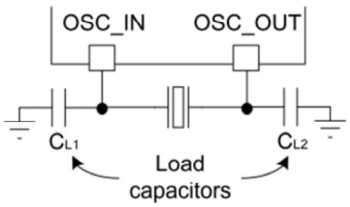
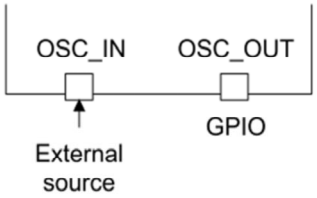
During and after reset, the alternate functions are not active, only debug pins can be used in Alternate Function mode.
Pin PA14 is shared with BOOT0 functionality. Caution is required as the debugging device can manipulate the BOOT0 pin value, which selects the boot mode.

Special considerations for HSE/LSI pins

- **Oscillator pins can be used as standard I/O pins**
  - When the oscillator is switched OFF, related pins behave as I/O pins
    - Valid for both HSE / LSE
    - This state is the default one after reset
  - When user external clock mode is used, the second pin behaves as an I/O pin
    - Only OSC_IN or OSC32_IN is used as clock source
    - OSC_OUT and OSC32_OUT are standard I/O pins





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When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.
When the external clock source is used instead of a crystal oscillator, only the related OSC_IN pin is used for the clock and the OSC_OUT pin can be used as a standard I/O pin.

Multi-supply I/O pins

- **Some I/O pins can be supplied from different sources**

- New I/O pin supply scheme brings new I/O pin structures and names
  - FT (Five Volt Tolerant) definition is extended by new abbreviation suffix
  - Maximum VIN is defined by lowest supply voltage connected to the structure of given I/O pin
  - For example, formula $V_{IN} < \min (V_{DD}, V_{DDA}) + 4.0$ V applies for FT_a pin

Abbreviation suffix	Description	Example
_f	**I/O with Fm+ capability, supplied by VDD** ➢ Fast-mode Plus (Fm+) bit rate of up to 1 Mbit/s and extra output drive I/Os	FT_f
_a	**I/O with analog switch function, supplied by VDDA**	FT_a
_c	**I/O, USB Type-C PD capable**	FT_c

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A new multi-supply scheme of I/O pins brings new I/O pin structures. Previously-used naming – FT (Five Volt Tolerant) , TT (Three Volt Tolerant) – has been extended by abbreviation suffixes to highlight alternate supply sources for each FT and TT I/O pin.
Previously-used name FTf for Fm+ capable pins has been transformed to FT_f, suffix _a marks pins supplied by analog supply, suffix _c is used for pins supporting USB Type-C Power Delivery.
The absolute maximum rating for each I/O pin is defined by the lowest voltage of the supplies listed for each I/O pin.

Low-power modes

Mode	I/O Description
Run	Active.
Sleep	Active.
Low-power run	Active.
Low-power sleep	Active.
Stop 0	Active.
Stop 1	Active.
Standby	Only as input with internal pull-up, pull-down or floating. Configuration lost when exiting.
Shutdown	
Reset	Forced to analog input mode when the MCU is under reset.

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I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost. When the MCU is under reset, I/O pins are forced into an analog input mode.

STM32G0 limitation on GPIOs

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- Some GPIOs in the device have limited functionality linked to other internal features:
  - UCPD CC lines: These lines will present limited output speed
  - UCPD DB lines: The voltage level on these IO will enable potentially a pull down on the CC lines. To overcome this situation, 2 STROBE bits are present in the SYSCFG register and will allow the user to not see that effect.
  - VBAT domain GPIOs: Like on other devices, these IOs have a limited drive current capability.

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VBAT domain GPIOs: PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:

- The speed should not exceed 2 MHz with a maximum load of 30 pF
- These GPIOs must not be used as current sources (for example to drive an LED).